SECTION 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual contains descriptions, set-up and operating instructions, specifications, maintenance, and service information for the Telecommunications Techniques Corporation (TTC) Model 30678 DDS DS0A/B Data Interface. The DDS DS0A/B Data Interface allows the FIREBERD 6000 and 4000 mainframes to be connected to Digital Data System (DDS) circuits for DS0A, DS0B, and clear channel testing and analysis.

1.2 INTERFACE FEATURES

The DDS DS0A/B Data Interface has the following features.

- Controlled through the FIREBERD front panel interface set-up menu or from a remote terminal.
- Analyzes DS0A-formatted data (full duplex, synchronous data) at 2.4, 4.8, 9.6, 19.2, and 56 kb/s; DS0B-formatted data at 2.4, 4.8, and 9.6 kb/s; and DS0 64 kb/s clear channel data.
- Analyzes DDS secondary channel data for either DS0A- or DS0B-formatted data at any applicable rate.
- Provides an RS-232-C Interface which allows another FIREBERD Communications Analyzer or a protocol analyzer to simultaneously test either the primary or secondary channel.
- Establishes and maintains alternating loopbacks at OCUs, DSUs, CSUs (with or without local loop-repeaters), up to two 56 kb/s repeaters, and HL96NY terminals.
- Establishes latching loopbacks at compatible OCUs, CSUs, LSIs, MJUs, DS0-DPs, and DSUs.
- Generates a programmable data only, frame only, or data and frame bit error rate (fixed rate in the FIREBERD 4000).
- Establishes DDST loopback.
- Controls single or cascaded Multipoint Junction Units (MJUs).
- Tests integral subrate multiplexers (ISMX) or subrate data multiplexers (SRDM) by transmitting data in one format (DS0A or DS0B) and accepting data in another (DS0B or DS0A).
- Provides a byte encoder for testing circuit sensitivity to specific byte codes singly or continuously.
- Establishes an interface THRU mode for passing data through the interface without affecting the data (with or without error insertion).
- Samples and displays the received data bytes and identifies network control codes by name.

1.3 INTERFACE COMPATIBILITY

The DDS DS0A/B Data Interface is designed in consideration with the following publications and specifications.

- AT&T CB 126, April 1981, D3 and D4 56 Subrate Dataport Channel Unit Technical Reference and Compatibility Specification.

- AT&T CB 141, April 1981, D3 and D4 56 kb/s Dataport Channel Unit Technical Reference and Compatibility Specification.
- AT&T Communications Technical Reference PUB62120, April 1984, Digital Data System with Secondary Channel.
- AT&T Communications Technical Reference PUB62310, September 1983, Digital Data System Channel Interface Specification.
- Bellcore, TA-TSY-000055, Issue 3, April 1987, Basic Testing Functions for Digital Networks and Services.
- Bellcore, TA-TSY-000189, Issue 1, April 1986, Generic Requirements for the Subrate Multiplexer.
- Bellcore, TA-TSY-000192, Issue 2, April 1986, Digital Data System (DDS) Multipoint Junction Unit (MJU) Requirements.
- Bellcore, TR-NPL-000157, Issue 1, September 1985, Secondary Channel in the Digital Data System: Channel Interface Requirements.

1.4 OPTIONS AND ACCESSORIES

The following cables are available from TTC for the DDS DS0A/B Interface.

- Model 30488, 10' DS0 clock cable with 9-position D-type male to 5-pin female connectors (supplied with interface).
- Model 20309, 10' OIU adaptor cable with 9-position D-type male to 9-position D-type male connectors.
- Model 30611, 4' cable with 9-position D-type male to 5-pin male connectors.
- Model 30518, 14' cable with dual bantam plugs to 5-pin male connector.
- Model 10615, 10' bantam plug to bantam plug cable.
- Model 10648, 10' bantam plug to alligator clips cable.

SECTION 2
INTERFACE DESCRIPTION

2.1 INTRODUCTION

The DDS DS0A/B Data Interface is a menu controlled interface with no mechanical controls. This section describes the front panel connectors and functional descriptions of each interface capability and feature. All interface control is provided through the mainframe interface set-up menu or from a remote device. The DS0A/B Interface menu and remote control are described in Section 3 for the FIREBERD 6000 and Section 4 for the FIREBERD 4000.

2.2 PHYSICAL DESCRIPTION

The DDS DS0A/B Data Interface has clock (CLOCKS) and data (TX OUTPUT and RX INPUT) connections which allow the FIREBERD to connect to the DDS network (see Figure 2-1). The 25-pin connector (PROTOCOL PORT, DCE) provides full duplex access to unformatted primary or secondary channel data. The interface module slides into the rear panel interface slot in the FIREBERD and front panel slot in the interface extender unit (IEU), or ISU-6000.

NOTE: The FIREBERD 6000 Communications Analyzer requires Revision E software or greater to operate with the DDS DS0A/B Data Interface. All revisions of the FIREBERD 4000 operate with the interface.

2.2.1 Interface Clock Connection

The interface CLOCKS connector is a female, 9-pin, D-type, subminiature connector (see Figure 2-1). It provides input connections for logic and bipolar level bit (64 kb/s) and byte (8 kb/s) clocks. The clock level format is determined by the clock cable used. A clock cable (Model 30488) is supplied with the interface for connecting to 5-pin clock connectors. When combined with an adaptor cable (Model 30518), the clock cable permits access to separate bit and byte clocks through bantam jack connectors. An optional cable with 9-pin male-to-male connectors (Model 20309) is available to connect the FIREBERD to an office interface unit (OIU) in the D4 channel bank. The connector pin assignments are listed in Table 2-1.

Table 2-1
CLOCKS Connector Pin Assignments

Pin #	Description
1	Not connected
2	Signal ground
3	Logic level 64 kb/s bit clock input
4	Logic level 8 kb/s byte clock input
5	Signal ground
6	Bipolar 8 kb/s byte clock input (+)
7	Bipolar 8 kb/s byte clock input (-)
8	Bipolar 64 kb/s byte clock input (+)
9	Bipolar 64 kb/s byte clock input (-)

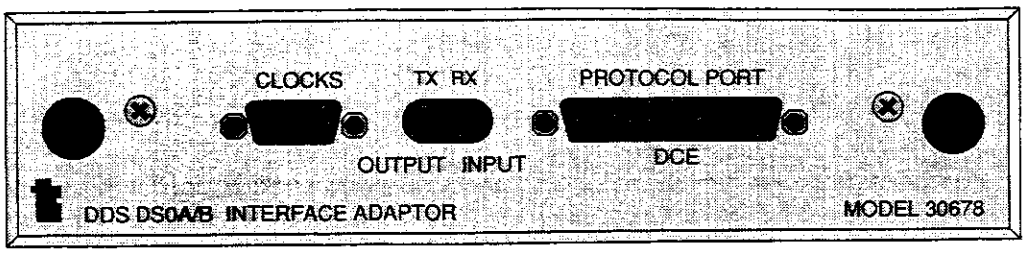

Figure 2-1
The DDS DS0A/B Data Interface

2.2.2 Interface Data Connections

The two interface data connections, labeled TX OUTPUT and RX INPUT, are bantam tip-ring-sleeve jacks. The jacks only accept bantam plugs. The RX INPUT jack can be terminated in the bipolar mode by grounding the jack sleeve lead. When the RX INPUT jack is terminated, the mainframe ALM1 LED illuminates. When the sleeve is not grounded, the RX INPUT can bridge an existing termination. Logic and bipolar signal formats are selectable through the DS0A/B Interface Connector menu. The bipolar signal which appears on the trip and ring jack lead is transmitted at ±5V. The interface can receive a bipolar signal from ±3.5 to ±5V. The bipolar signals are non-return-to-zero (NRZ) with alternate mark inversion (AMI) coding. The logic level signals appear on the tip jack leads when testing near-end circuits (LOGIC NEAR) and on the ring jack leads when testing the far-end circuits (LOGIC FAR). The logic signal level is 0V to +5V.

2.2.3 Protocol Port Connection

The DCE PROTOCOL PORT is an EIA RS-232-C, 25-pin, female connector that allows another FIREBERD or protocol analyzer to be connected to the interface for direct access to unformatted primary or secondary channel data. The auxiliary test set can transmit and receive data on the channel the FIREBERD is not testing. This permits simultaneous testing of both primary and secondary channels. RTS controls the port operation. When RTS is high, the port can transmit and receive data. When RTS is low, all Marks are substituted for port data. Table 2-2 lists the protocol port pin assignments.

Table 2-2
DCE PROTOCOL PORT Connector
Pin Assignments

Pin #	Abbrev.	Direction	Description
2	TD	Input	Transmit Data
3	RD	Output	Received Data
4	RTS	Input	Request to Send
5	CTS	Output	Clear to Send
6	DSR	+V	Data Set Ready
7	SGND	—	Signal Ground
8	RLSD	+V	Received Line Signal Detect
15	SCT	Output	Serial Clock Transmit
17	SCR	Output	Serial Clock Receive

RS-232-C compatible and configured as the DCE.
Pins 6 and 8 are internally tied high.

2.3 FUNCTIONAL DESCRIPTION

The DDS DS0A/B Data Interface provides the FIREBERD 6000 and 4000 Communications Analyzers with the ability to test and analyze Digital Data System (DDS) circuits at the DS0A and DS0B levels and 64 kb/s clear channel. With the DDS DS0A/B Interface, the FIREBERD can test the DDS network in a straightaway test with another FIREBERD or KS-type test set, or by itself with the network loopback capabilities. The following information provides a functional description of the clock and data signals, test modes, and capabilities of the interface.

2.3.1 Data and Clock Signals

All signals between the FIREBERD and DDS network are made through the DDS DS0A/B Interface. The DDS DS0A/B Interface operates with full duplex, synchronous data. The test data patterns are transmitted from the TX OUTPUT jack in either a DS0A or DS0B bipolar or logic level signal format at data rates of 2.4, 4.8, 9.6, 19.2, 56, and 64 kb/s. The RX INPUT jack accepts the DS0A or DS0B data from the DDS network for analysis at the same signal levels and data rates as the TX OUTPUT jack. Not only does the DDS DS0A/B Interface test and analyze the primary data channel, it also provides the capabilities to test the DDS secondary channel.

The bit (64 kb/s) and byte (8 kb/s) clocks are provided to the FIREBERD through the CLOCKS connector on the interface. The DDS bit and byte clocks supplied to the interface synchronize the interface and mainframe to the DDS network data and clocks for normal operation.

NOTE: The bit and byte clock signals must be supplied to the interface for all interface operating modes, including the mainframe SELF LOOP.

2.3.2 DS0A Channel Testing

When configured for DS0A operation, the interface formats the test pattern with the appropriate frame and control bits and byte stuffing format (as required) to bring the data rate up to the 64 kb/s rate. When the interface is operating at 19.2 kb/s, the front panel frame synchronization LED (FRM SYNC on FIREBERD 6000 and FRAME SYNC on FIREBERD 4000) illuminates indicating that the interface has synchronized with the received 19.2 kb/s framing pattern (01100). Once synchronized to the incoming signal, framing errors and other results are available.

2.3.3 DS0B Channel Testing

The interface can test DS0B signals and associated framing at 2.4, 4.8, and 9.6 kb/s on any one of up to 20 channels. The subrate used determines the number of available channels for which the subrate multiplexer is configured, i.e., 2.4 kb/s allow 20 channels, 4.8 kb/s allow 10 channels, and 9.6 kb/s allows 5 channels. When testing the DS0B channel, the test data is placed in the selected DS0B channel and the Unassigned Multiplex Channel (UMC) code is placed on the remaining channels. The subrate framing pattern within the DS0B signal identifies the subrate and number of customer signals or channels that are multiplexed into a single DS0B signal operating at 64 kb/s. The DS0B framing patterns are shown in Table 2-3 for each subrate and DS0B multiplexer configuration.

Table 2-3
DS0B Framing Patterns

Channels	Rate	Bit Pattern
1 to 5	9.6 kb/s	01100
1 to 10	4.8 kb/s	01100 10100
1 to 20	2.4 kb/s	01100 10100 11100 00100

The interface acquires frame synchronization after two complete unerrored framing patterns are detected. When DS0B frame synchronization has been achieved, the front panel frame synchronization LED (FRM SYNC on FIREBERD 6000 and FRAME SYNC on FIREBERD 4000) illuminates. Once framing synchronization has occurred, the FIREBERD monitors the framing and data patterns and reports inconsistencies in the mainframe analysis results display.

2.3.4 64 kb/s Clear Channel Testing

Pressing the CLRCH mode softkey automatically configures the interface for 64 kb/s clear channel operation. Data is then transmitted and received within the full 8-bit byte. Since there is no control bit, control commands such as loopbacks cannot be enabled. Test data generated by the mainframe is transmitted and received at 64 kb/s without control and framing bits. It should be noted that the BYTE encoder is disabled during clear channel operation.

NOTE: According to DDS circuit specifications, no more than seven consecutive zeros may be transmitted per data byte. Use the appropriate fixed (MARK, 1:1, or 1:7) or pseudorandom (63 or 511) test patterns to accomplish this requirement.

2.3.5 Primary and Secondary Channel Testing

In some DDS networks, a primary data channel and a secondary low-speed data channel are available to the customer. The DDS secondary channel provides the customer with the ability to communicate, manage, and test the network without interrupting the primary data channel. The secondary channel is made available by time-sharing every third control bit (bit 8) of the main data stream. The FIREBERD can test and analyze the secondary channel from the DS0A/B Interface with all modes except clear channel.

Both channels can be tested through the DS0A/B Interface, one at a time by the FIREBERD or simultaneously with a test instrument connected to the interface PROTOCOL PORT. The auxiliary CHAN menu controls which DDS channel the FIREBERD is testing. Pressing the PRI (primary) or SEC (secondary) softkey switches the FIREBERD between the channels. Normally, the FIREBERD transmits and receives data over the primary channel, while the secondary channel can be accessed through the PROTOCOL PORT. However, if the secondary channel is not provided, the PROTOCOL PORT can still be used to analyze the primary channel by changing the auxiliary CHAN menu to SEC. In this configuration, the mainframe MARK test pattern should be selected.

When testing the secondary channel with either the FIREBERD or an external analyzer, DDS data restrictions described in the AT&T PUB62120 and Bellcore TR-NPL-000157 publications must be observed. Only the 511- and 2047-bit pseudorandom test patterns meet these restrictions. Using other patterns might not produce the correct results.

The measured bit error rate indicated by the mainframe may actually be higher than the actual bit error rate of the secondary channel. This occurs because of the coding scheme of secondary channel. The normal secondary channel data rates are related to the primary channel data rate as follows:

PRIMARY CHANNEL DATA RATE	SECONDARY CHANNEL DATA RATE
2.4 kb/s	0.133 kb/s
4.8 kb/s	0.266 kb/s
9.6 kb/s	0.533 kb/s
19.2 kb/s	1.066 kb/s
56 kb/s	2.666 kb/s

2.3.6 Loopback Testing

The interface can test the DDS network using two loopback modes: alternating and latching. The interface allows either mode to be selected along with a number of selectable terminal loopbacks. Once the loop is established, the FIREBERD sends test patterns out to test and analyze the circuit between the FIREBERD and the looped terminal. The loopback tests can be performed in all modes but the MUXTST mode.

ALTERNATING LOOPBACK MODE

The interface enables the FIREBERD to test DDS networks from a single point of reference by establishing alternating loopbacks at one of several locations like those shown in Figure 2-2. Refer to Section 3.4.4 for a complete list of alternating loopbacks generated by the interface.

The Alternating Loop menu provides the nine loopback selections which can loop a single terminal even when another device is between the mainframe and the looped terminal. This is very helpful for instance, when establishing a channel (CSU) loop on a 56 kb/s circuit with local repeaters.

NOTE: Alternating loopback tests cannot be performed when testing the DDS secondary channel.

NOTE: Alternating loopback is synonymous with non-latching loopback.

The selected alternating loopback sequence (press the TYPE softkey) is transmitted when the mainframe LOOP UP switch is pressed. When the mainframe has synchronized with the returning loop code, the mainframe CODE LED illuminates and data and framing analysis begins. During the loopback test, the loop code and test pattern bytes are transmitted alternately. The sequence continues until either the LOOP DOWN switch is pressed or the sequence is interrupted. The appropriate test pattern can be generated using the mainframe pattern generator. During the loop-up and loop-down sequences, the mainframe displays messages indicating the progress of the sequence. A list of the displayed alternating loopback status messages is provided in Appendix B.

NOTE: Do not use the interface byte encoder when using alternating loopbacks.

When using alternating loopback procedures, the RCV FREQ results display indicates one-half the actual data rate. The mainframe only analyzes the received test pattern and not the combined loop code and data.

Latching Loopback Mode

The interface enables the FIREBERD to test DDS networks from a single point of reference by establishing latching loopbacks at one of several locations, like those shown in Figure 2-3.

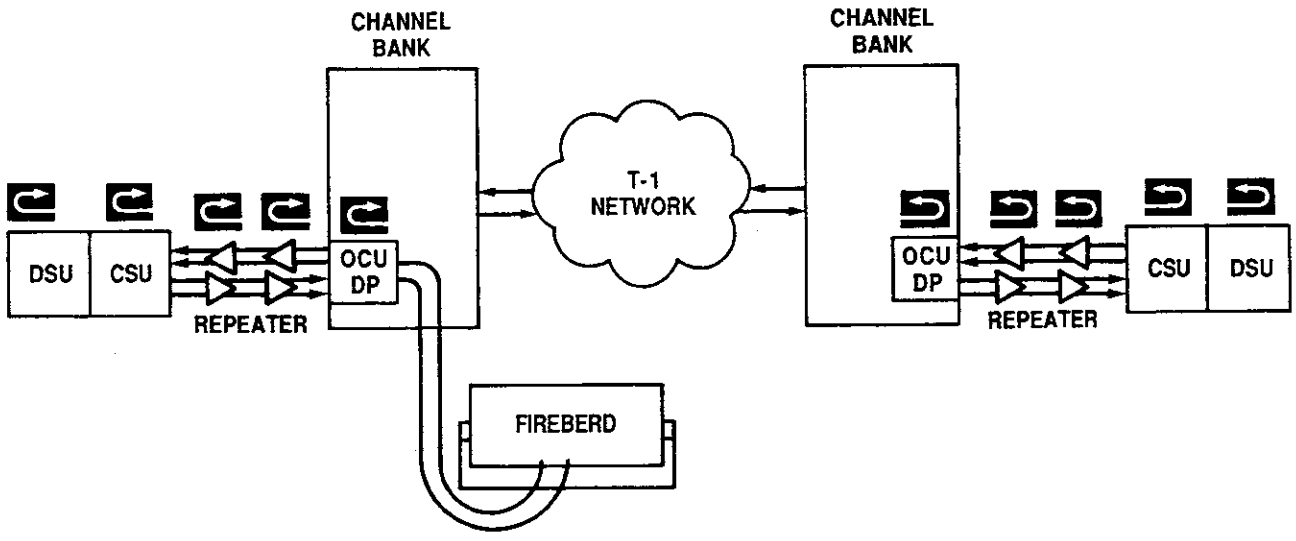

Figure 2-2
DDS Alternating Loopback Locations

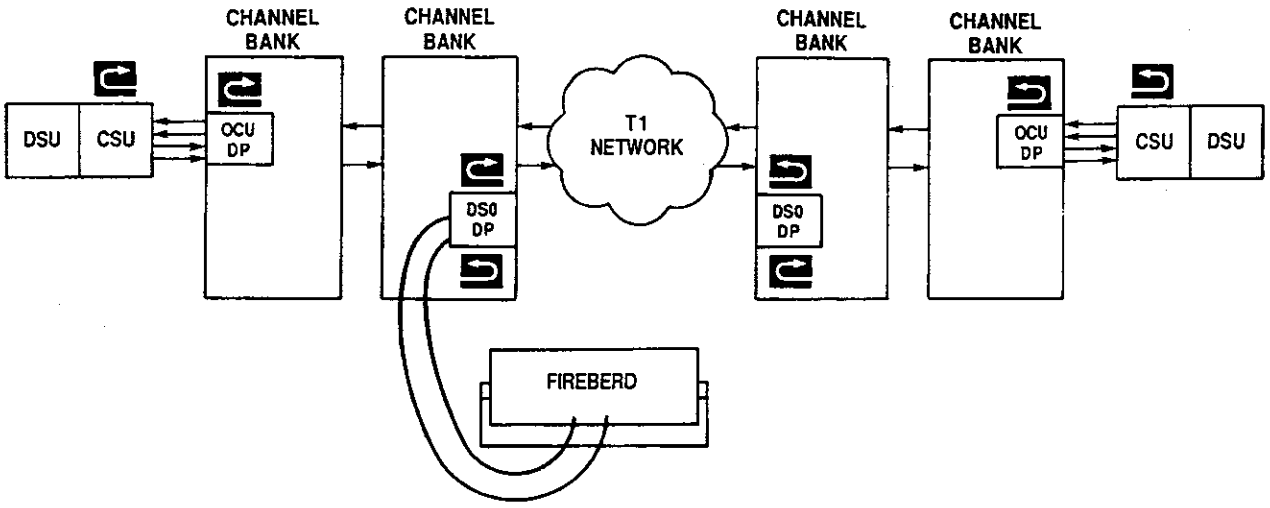

Figure 2-3
DDS Latching Loopback Locations

The Latching Loop menu provides the latching loopback selections that can loop a single terminal capable of responding to the appropriate latching loop codes. The selected latching loopback (use the TYPE and LOC softkeys) sequence is initiated by pressing the mainframe LOOP UP switch. When the loop is established and the confirmation code is received, the loopback is reported as successful and a confirmation message is displayed. The loop-down sequence (press mainframe LOOP DOWN switch) disables the loop.

During loop-up and loop-down sequences, the mainframe displays messages indicating the progress of the sequence. When a MJU loopback is established, the confirmation message also displays the MJU HUB ID number. A list of the displayed latching loopback status messages is provided in Appendix B.

When testing DS0-DPs, the confirmation message may also include the direction of the established loop by displaying "MAP0 line side" or "MAP1 drop side". The MAP0 confirmation code indicates that a loopback was achieved on the DS0-DP line side. The MAP1 confirmation code indicates that a loopback was achieved on the DS0-DP drop side. If no MAP code is reported by the DS0-DP, no additional information is displayed with the confirmation message. Up to eight DS0-DP locations (a location being the drop or line side of the DS0-DP) can be identified by pressing the LOCATN softkey (1-8) before sending the loop (up or down) code.

2.3.7 DS0B Subrate Multiplexer Testing

Another capability of the interface is DS0B subrate multiplexer testing (MODE, MUXTST). The interface allows the mainframe to test ISMXs and SRDMs by transmitting a DS0A- or DS0B-formatted test signal into one side of the multiplexer (input) and receiving the opposite format from the other side of the multiplexer (output). Figure 2-4 shows the FIREBERD connected to the SRDM.

The subrate multiplexer can be tested by passing a test pattern from the mainframe or BYTE encoder through the multiplexer and analyzing the results. Refer to Section 2.3.3 for additional information on DS0B channel testing.

NOTE: The mainframe SELF-LOOP test cannot be performed on the interface in the MUXTST mode

2.3.8 Multipoint Network Control and Testing

The FIREBERD can access, control, and test single or cascaded MJUs. The auxiliary MJU menu provides the FIREBERD with the ability to select the MJU branch (1-4), block or unblock a branch, release all branches from all MJU commands, and restore selected branches in the network. The MJU controls are provided for two reasons: (1) to block a branch from interfering (e.g., streaming) with normal network operation and (2) to select a remote branch for testing.

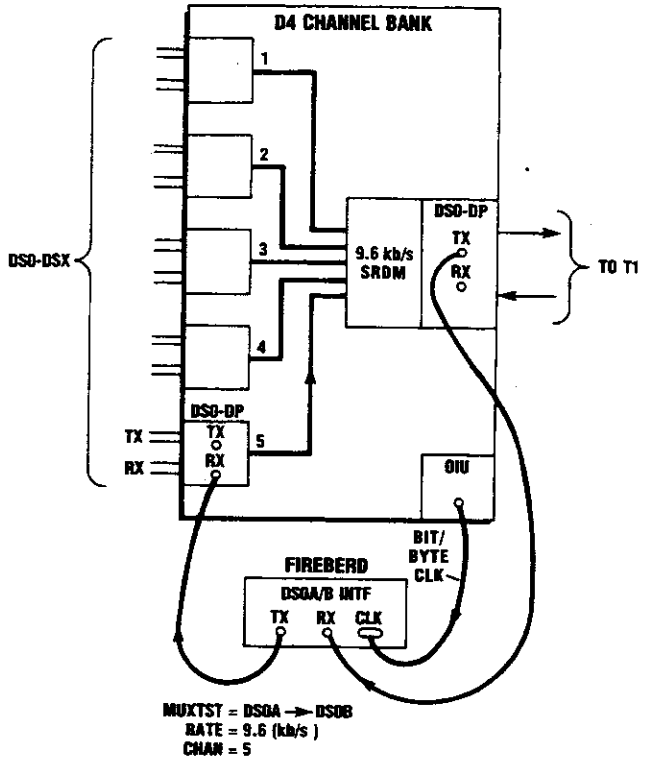

Figure 2-4
Testing Subrate Multiplexers

MJU Control Commands

To gain access and control over a branch, it must be selected. The MJU branch select sequence involves pressing the BRANCH softkey to identify the branch (1-4), then pressing the SELECT softkey to transmit the code sequence to the MJU. This connects the control channel to the selected branch and blocks the other branches. This makes the MJU transparent to the next branch select sequence or loopback test signals which would be transmitted down the branch to the next terminal (e.g., MJU or CSU). If a branch is not selected, the signal is transmitted on all unblocked branches. In networks with cascaded MJUs, repeat the branch select sequence to bypass any cascaded MJUs to reach the terminal being tested. Figure 2-5 shows a MJU configured in a branched state. When the branch select sequence is executed, the MJU reports its position in the network with the HUB ID number. When the select sequence is successful, the received HUB ID and selected branch number are displayed in the results display. The available MJU status messages are listed in Appendix B.

Once the branch is selected, the other MJU commands control the condition of the branch. When the BLOCK softkey is pressed, the block command is detected by the MJU and the selected branch is disconnected from the network (the other branches are restored). Figure 2-5 shows a MJU configured in a blocked state. If the selected branch is blocked, sending the unblock command (press UNBLK softkey) unblocks it and restores the other branches. To return the selected branches back to normal operation, press the RESTOR softkey. The restore command returns the MJU to normal operation without releasing the blocked branches (those blocked by the BLOCK command). The MJU release command (press the RELEAS softkey) releases all test modes and blocked and selected branches on all MJUs downstream within the multipoint network.

MJU Loopback Control

In a multipoint network, loopbacks must be established from the upstream side of the MJU. To test a terminal (e.g., DS0-DP, OCU-DP, or CSU) on the downstream side of the MJU, the appropriate MJU branch must be selected first (refer to MJU Control Command). Attempting to establish an upstream loopback from the downstream side of the MJU does not properly prepare the network for testing. The MJU itself may be looped using a latching loopback command. This is done through the Latching Loopback menu. Figure 2-5 shows a MJU configured in a latching loopback state.

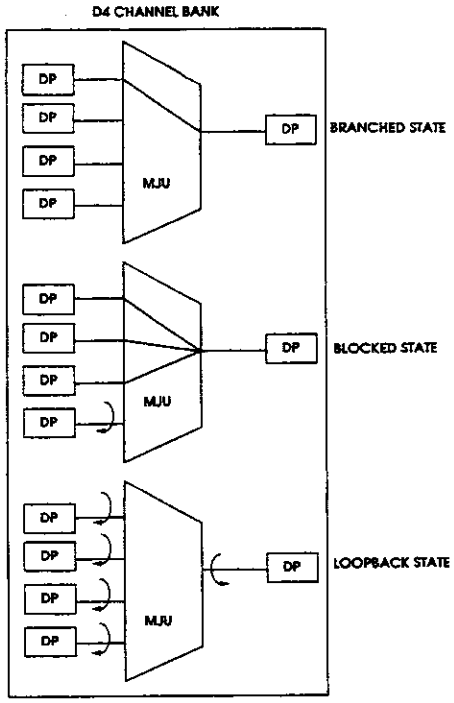

Figure 2-5
Multipoint Junction Unit Test States

2.3.9 Interface Byte Encoder

The DDS DS0A/B Interface provides a programmable 8-bit byte encoder that allows single or repeated transmission of any 8- bit byte sequence. The byte encoder can be used to transmit control codes and alarms. Commonly used control codes are listed in Appendix A. When the interface is configured for DS0A 19.2 kb/s or DS0B operation, bit 1 of the byte encoder is overwritten with the appropriate framing pattern.

When the SINGLE softkey is pressed, OFF is replaced with SINGLE in the upper right corner of the display once the code is sent. To send the code continuously, press the REPEAT softkey. In the repeat mode, turn the encoder off by pressing the OFF softkey. The HELP softkey (FIREBERD 6000 only) explains the constraints on the code entered, i.e., enter 8-bit binary code.

NOTE: When the encoder is active, the mainframe test pattern function is disabled. Also, the encoder cannot be used in the THRU mode, during alternating loopback tests, or during 64 kb/s clear channel testing.

2.3.10 Interface THRU Mode

The THRU mode places the interface in a transparent mode which allows the FIREBERD to be placed in series with the network. The interface loops the received data entering the RX INPUT jack to the TX OUTPUT jack as the transmit data. The mainframe cannot transmit its own test patterns during the THRU mode. However, the mainframe can still analyze the received data. The looped data can be altered by injecting a specified error rate from the interface error rate generator.

NOTE: The mainframe transmitter and interface byte encoder are disabled when using the THRU mode.

2.3.11 Interface ERROR Rate Generator

The DDS DS0A/B Interface contains a programmable bit-error-rate generator that is accessible through the DS0 A/B Interface menu. The generator can be activated on all transmitted signals regardless of the data source (e.g., mainframe test pattern, interface byte encoder, or THRU mode). On the FIREBERD 6000, the interface error rate generator supplements and operates

independently of the mainframe ERROR INSERT switch by providing a range of error rates that are entered using the mainframe keypad. The FIREBERD 4000 provides a fixed rate of 1E-6. The error rate can be programmed to have an effect only on data bits, only on framing bits, or on both data and framing bits at the same time. Unpredictable error rates can occur when both mainframe and interface error rate generators are used at the same time.

NOTE: The FIREBERD 6000 controls the generator output rate and should be set for 64 kb/s to maintain a match between the displayed and actual error rate being generated. Other frequencies can be used but the generator error rate does not match the displayed rate. On the FIREBERD 4000, the clock generator is automatically set for 64 kb/s.

2.3.12 Interface Protocol Port

The PROTOCOL PORT is an RS-232-C DCE configured interface that allows an external device to transmit and receive unformatted data through the DS0A/B Interface to and from the DDS network over the primary or secondary DDS channel. The interface provides the necessary DDS-to-RS-232 data conversion between the DDS network and the PROTOCOL PORT. This data conversion allows the port to operate at the selected DS0, DS0A, DS0B, or secondary channel data rate. When the PROTOCOL PORT is inactive (RTS is low), all 1's replace the transmit data on the selected channel. Any device connected to the PROTOCOL PORT must use the clocks provided by the port for both transmit and receive directions. The DSR (Pin 6) and RLSD (Pin 8) leads are permanently set high.