Development of a Two-Channel Frequency Synthesizer

Combining two independent synthesizers, flexible modulation, and control circuits in a single package, this instrument can generate two-phase, two-tone, pulse, frequency hopping, and swept signals.

by Michael B. Aken and William M. Spaulding

AS THE COMPLEXITY of electronic circuits and systems has increased, the need for equally complex, high-quality test signals has grown. In response to the need for greater flexibility, Hewlett-Packard has developed the HP 3326A Two-Channel Synthesizer, Fig. 1. This instrument is based on the same fractional-N synthesis technique used in the HP 3325A Synthesizer/Function Generator,[1] which was introduced in 1978. The addition of a second synthesizer and output channel, all under the control of a common microprocessor, has resulted in a high-performance signal source that has operational features extending well beyond the direct combination of two independent signal sources.

Frequency coverage is from dc to 13 MHz with one-microhertz resolution below 100 kHz and one-millihertz resolution from 100 kHz to 13 MHz. Output levels are programmable from 10V p-p into 50Ω (23.98 dBm) to 1 mV p-p (−56.02 dBm) with 0.01-dB resolution. Independent preattenuator dc offset can be applied to the output signals. Functions available include dc-only, and there is independent control of the selected function on each output channel. The article on page 19 gives examples of the applications of the HP 3326A.

Functional Modes

The HP 3326A has four modes of operation: two-phase, two-channel, two-tone, and pulse.

Two-phase operation. In this mode, high-accuracy phase control is provided by Hewlett-Packard's implementation of fractional-N synthesis. Two synthesizers and two chains of output circuitry are combined to provide continuous phase control between the output channels over a range of ±720° with 0.01° resolution. An internal calibration system working through the instrument's controller provides fully calibrated phase between the output channels across the full frequency range of dc to 13 MHz. Waveforms may be sinusoidal, square, or mixed sine and square. The calibration system can be used to provide multichannel phase operation among several instruments for output frequencies greater than 1 kHz. Multiphase operation at lower frequencies can be achieved with the addition of a time-interval counter and a computer to act as system controller. Phase is not calibrated when using the HP 3326A's optional high-voltage amplifiers, since they are connected after the output attenuators outside the calibration path. High-voltage phase accuracy can be enhanced using an external time-interval counter such as the HP 5334A.

Fig. 1. *The HP 3326A Two-Channel Synthesizer can generate either two independent signals or a combination of the signals in its two channels. Each channel produces sine and square waves from 1 μHz to 13 MHz with separately controllable amplitude and dc offset. Pulse and flexible modulation capabilities are built-in.*

Two-channel phase performance is complemented by excellent sinusoidal signal purity. Harmonically related products are more than 80 dB below the carrier from 10 Hz to 50 kHz. Nonharmonically related spurious signals are greater than 80 dB down below 1 MHz and greater than 70 dB down from 1 MHz to 13 MHz. Phase performance specifications apply for equal and unequal levels between channels, for a sine/square waveform mix between channels, and for waveforms with dc offset.

Two-channel operation. In the two-channel mode, the HP 3326A functions as two independently programmable frequency synthesizers. Sweep time and sweep marker are the only parameters shared by both channels. Channels can be independently set to sinusoidal, square, or dc-only waveforms. The same harmonic and spurious specifications apply as in the two-phase mode.

Two-tone operation. In the two-tone mode, the frequency of Channel B tracks the frequency of Channel A with a programmable offset of up to ±100 kHz. Using the frequency sweep features of the instrument, tracking swept two-tone measurements may be made. Independent control of waveforms, amplitudes, and dc offsets is maintained in each channel.

Pulse generation. With two channels having precise phase control, it was a natural extension to provide pulse generation using the equivalent of a set/reset flip-flop triggered on the rising edges of the two phase-related sinusoids. As the phase of Channel B is varied with respect to Channel A over a range of 0 to 360°, pulses with precisely controlled duty cycles from 1 to 99% can be generated with a repetition frequency equal to the programmed frequency of Channel A. The complementary outputs of the square modulator are delivered to the output amplifiers to provide pulses 180 degrees out of phase on the two channels. Independently programmable dc offsets can be applied to the pulse waveforms.

Operating Features

Versatile modulation capabilities are built into the HP 3326A Two-Channel Synthesizer. Rear-panel inputs are provided for external amplitude and phase modulation of the two output channels. Internal modulation is provided by routing the signal from Channel B to the amplitude and/or phase modulation circuits of Channel A. Amplitude modulation rates up to 100 kHz and depths from 0 to 100% are allowed. Phase modulation is accomplished within the fractional-N phase-locked loops. Rates to 5 kHz and peak deviations to ±360° are possible. Modulation percentages and/or deviations are fully programmable in the internal modulation mode.

The linear frequency sweep capabilities of the HP 3325A Synthesizer/Function Generator are maintained in the HP 3326A. Except for sweep time and frequency marker, all sweep parameters are independently programmable for the two output channels. Sweep capabilities have been extended in the HP 3326A with the introduction of discrete frequency sweep (see box, page 15). In this sweep mode, up to 63 sequential sweep elements, consisting of frequency pairs for Channel A and Channel B and the dwell time before moving to the next element, can be programmed. All frequency changes are phase-continuous. Simulation of DTMF (dual-tone, multifrequency) signals, such as those used for telephone dialing systems, and FSK (frequency-shift keying) for modem testing can be implemented directly with the HP 3326A.

The power of the internal microprocessor has been used to provide extensive calibration and self-test capability. Internal automatic calibration of amplitude, phase, phase modulation angle, and dc offset is provided. Fifty tests of internal circuitry are provided in firmware to verify the instrument's condition. Many of these tests are performed at instrument turn-on. Others are accessed during service and troubleshooting procedures. In addition, calibration error constants for most parameters are stored internally and used to correct entered data to enhance the accuracy of the instrument.

Especially useful in the two-tone mode is an integral resistive signal combiner, which can be used to provide both tones on a single output connector. Low-output impedance high-voltage amplifiers for both channels are offered as an option. These amplifiers provide up to 40 volts peak to peak (into a 1000Ω, 200-pF-maximum load) at frequencies up to 1 MHz with voltage-source drive. A high-stability crystal reference oven option is also available.

Block Diagram

The functional blocks of a mix-down synthesized signal source appear twice in the block diagram of the HP 3326A Two-Channel Synthesizer, Fig. 2.

Synthesized square waves (ECL levels) from the main fractional-N synthesizer are routed to the Channel A output mixer and to the RF switch. The Channel A mixer heterodynes a level-controlled, fixed 20-MHz signal from the reference dividers with 20 to 33 MHz from the main fractional-N synthesizer in all functional modes. Block diagram flexibility stems from the RF switch, which configures the Channel B output mixer frequency scheme to provide the functional modes. Fig. 3 describes the Channel B mixing frequency schemes for the four operating modes (two-channel, two-phase, two-tone, and pulse).

In the two-channel mode, the mixing scheme of Channel B is configured like that of Channel A. Leveled, fixed-frequency 20-MHz signals are applied to the mixer low-level port, with the auxiliary fractional-N synthesizer applied to the high-level port. Channel B can then be programmed to operate as a separate synthesizer output channel over the full 13-MHz range. In the two-phase mode, the auxiliary fractional-N synthesizer is connected to the Channel B mixer low-level port. The auxiliary fractional-N synthesizer runs at a fixed frequency of 20 MHz, with a phase angle (with respect to the 20-MHz Channel A signal from the reference) that is programmable using the phase control features of the fractional-N synthesis technique. Both channels operate at the same frequency, which is controlled by the main fractional-N synthesizer across the 0-to-13-MHz output range.

Two-tone operation is provided by programming an offset frequency in the auxiliary fractional-N synthesizer. Signals of 20 MHz plus or minus zero to 100 kHz from the auxiliary fractional-N synthesizer are routed to the Channel B mixer low-level port. Tones separated by up to 100 kHz over the 13-MHz range are developed in the output channels. Tone phase can be controlled with the auxiliary frac-

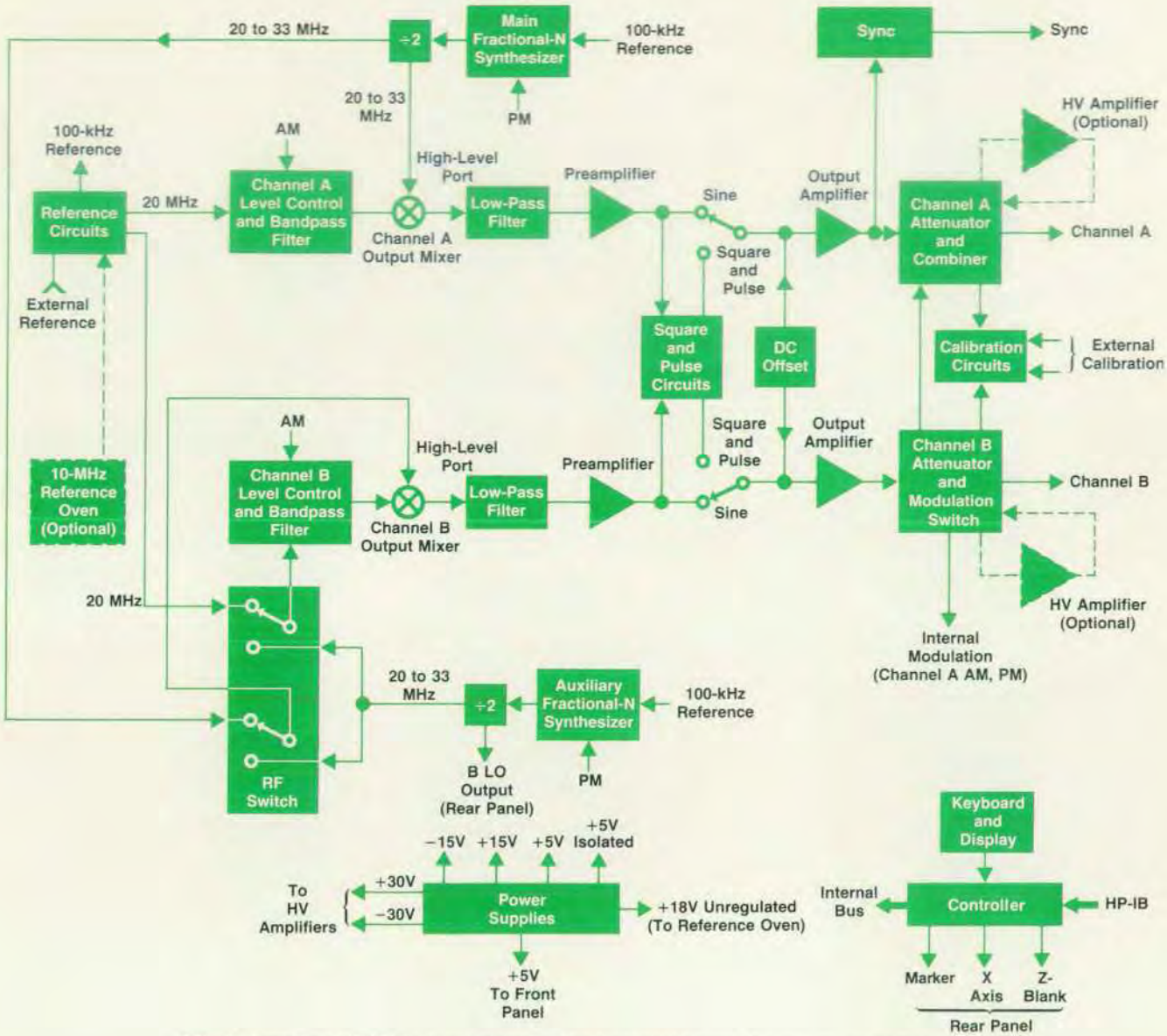


Fig. 2. *Simplified HP 3326A block diagram. The functional blocks of a mix-down synthesized signal source appear twice. Fractional-N synthesis provides high-accuracy phase control.*

tional-N synthesizer for harmonic relationships.

Pulse mode uses the same mixer configuration as two-phase mode. Preamplifier output sinusoids are shaped in the square and pulse circuits. A set/reset flip-flop, triggered by the edges of the two channels, generates the pulses, with duty cycle control established by varying the phase between the Channel A and Channel B signals. Level-controlled pulses 180° out of phase are then supplied to the output amplifiers.

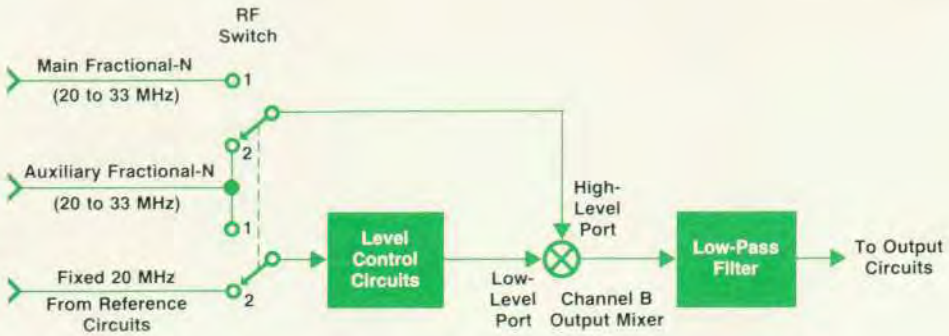
Square waves are generated by limiting the sinusoidal preamplifier outputs and applying them to level-control modulators. The modulator outputs are routed directly to the output amplifiers.

Sync circuitry subtracts any programmed dc offset from the Channel A output waveform. Fast comparators shape the signal to TTL levels, which are supplied to a front-panel connector.

Output attenuators provide 0 to 70 dB of programmable fixed attenuation for both channels. Fine amplitude control over a 10-dB range in 0.01-dB steps is accomplished with a 12-bit digital-to-analog converter in the level-control circuits for the individual channels. A resistive combiner is supplied on the Channel A output attenuator assembly to provide the convenience of two-tone outputs at a single front-panel connector. Combiner insertion loss is 6 dB and characteristic impedance is 50Ω.

External amplitude modulation signals from rear-panel connectors can be connected to the modulators for both output channels. Channel A can be amplitude and/or phase modulated by the signal from Channel B. Modulation signal switching is controlled by the microprocessor.

During calibration procedures, the attenuator outputs are disconnected from the front-panel connectors and routed to the calibration circuits.



Instrument Mode	RF Switch Position	Auxiliary Fractional-N Frequency Range
Two-Channel	2	20 to 33 MHz
Two-Phase	1	20 MHz
Pulse	1	20 MHz
Two-Tone	1	20 MHz ±(0 to 100 kHz)

Fig. 3. *HP 3326A Channel B output mixer RF signal switching.*

Fractional-N Synthesizers

Fractional-N frequency synthesis is an extremely powerful technique for signal generation with high-resolution frequency control.[1,2] It is used either directly or as an interpolation oscillator in many of the recent Hewlett-Packard swept-heterodyne analyzers and synthesized signal sources to implement local oscillators and/or output signals that are inherently stable, programmable, and easily swept. The HP 3326A is an excellent example of the versatility and adaptability of this synthesis technique.

Standard divide-by-N phase-locked loop synthesis, represented by the block diagram shown in Fig. 4, gives output frequencies that are integer multiples of the input reference frequency. High resolution in frequency demands the use of very large N numbers. However, for most applications the reference phase noise multiplication associated with large N is an unacceptable performance limitation.

Fractional-N techniques result in high-resolution frequency synthesis in a single phase-locked loop (Fig. 5, page 16). Here, the output frequency is N.F times the input frequency, where the fractional part (F) of the multiplier is composed of 12 BCD digits in the HP implementation. Phase noise multiplication is significant only for the integer part (N) of the multiplier, resulting in vastly improved performance over any other single-loop configuration with similar frequency resolution.

Since the counter output in the fractional-N loop is not an integer multiple of the reference frequency, the loop phase detector output contains a phase ramp with a period proportional to the fractional frequency offset. This ramping phase, if uncorrected, would result in very large phase modulation sidebands on the output frequency. To correct these sidebands, a digital phase accumulator in the control chip (an HP custom MOS chip) is updated with the fractional part of the frequency every reference cycle. The five most-significant digits of this accumulator feed a multiplying digital-to-analog converter (DAC), which provides a current ramp to the loop integrator to cancel the effect of ramping phase at the phase detector output. Sideband cancellation can be achieved to −130 dBc referred to the phase detector input.

Another benefit derived from the digital phase accumulator is precision control of phase in the phase-locked loop. By adding a constant to the contents of the accumulator in the control chip, the VCO phase with respect to the reference frequency can be varied with a theoretical resolution of 10 parts per million at the output frequency. This results in a phase resolution of 0.0036° using the five most-significant accumulator digits and the multiplying DAC. Phase control resolution in the HP 3326A is rounded to 0.01° for convenience.

Frequency sweep features have also been incorporated in the custom control chip. By adding a programmed frequency increment to the frequency register in the chip every reference cycle (10 μs), the loop output frequency can be swept. Flags generated on the control chip with digital comparators provide frequency marker and sweep limit indications (e.g., end of sweep).

Spectrally pure frequency systhesis is required for signals to be specified with accurate phase relationships. Spurious responses, harmonic distortion, and phase noise alter zero crossings. The HP 3326A implementation of fractional-N synthesis emphasizes spectral purity. Several circuit improvements are aimed directly at establishing performance consistency or improving performance.

Bias and API (automatic phase interpolation) current source temperature coefficients are stabilized to maximize

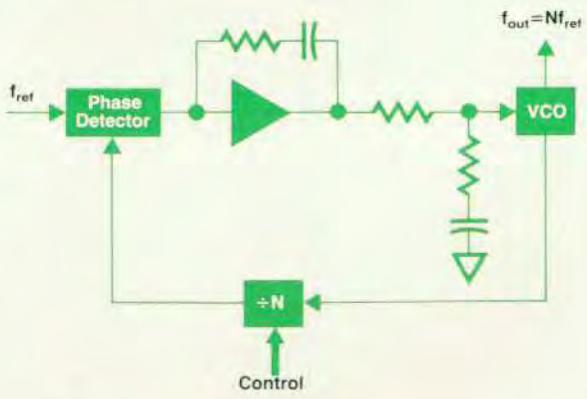


Fig. 4. *Conventional ÷N phase-locked loop block diagram.*

Discrete Sweep

Since the days of the first oscillator, user expectations have been increasing. The most important requirements are frequency accuracy, speed of frequency setting, and phase continuity. The synthesizer provided the frequency accuracy, while keyboards and the HP-IB brought local and remote programming. HP fractional-N frequency synthesis realized a glitch-free phase response. Now, the HP 3326A Two-Channel Synthesizer with its discrete sweep feature gives the user the ability to program a sequence of frequencies and the timing associated with each step of the sequence. Signals necessary for synchronization are also generated. Discrete sweep in the HP 3326A allows the user to program a series of 63 elements, each consisting of a frequency pair (Channel A and Channel B) and a dwell time. Once the frequencies and dwell times have been programmed, the user can recall or change each individual element, sweep continously through the programmed series of frequencies, or single-sweep the series. Dwell time is the interval between programming the individual local oscillators and the subsequent programming for the next element. It is limited to a range of values between 5 ms and 1000 s. Frequency settling time for the HP 3326A depends on the frequency step size. For large frequency steps the dwell time must be adjusted to allow for settling time. Although the technique is useful in the two-channel mode, its major contribution is in the other three HP 3326A modes. There, phase continuity is maintained between both of the local oscillators, phase repeatability is certain, and phase accuracy is exact at the particular frequency where the HP 3326A has been calibrated. A discrete sweep can be made in any of the four modes of operation. Since amplitude, offset, calibration, and function parameters are not stored with each discrete sweep element, the parameters used during the sweep are those in effect when the sweep is started. The operating mode chosen when the discrete parameters are programmed is remembered and cannot be changed without reentering the frequency and time parameters.

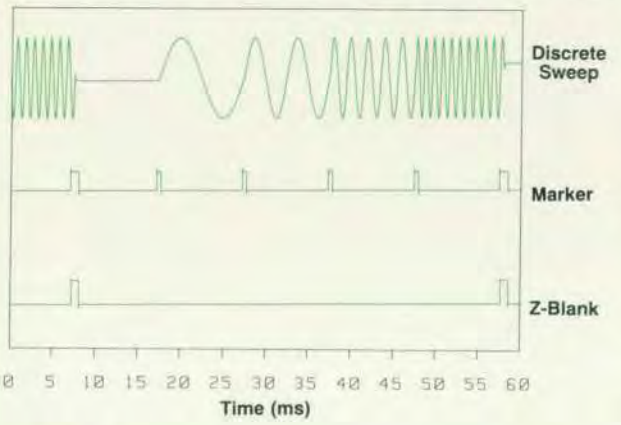


Fig. 1. *A discrete sweep with timing signals produced by the HP 3326A Two-Channel Synthesizer.*

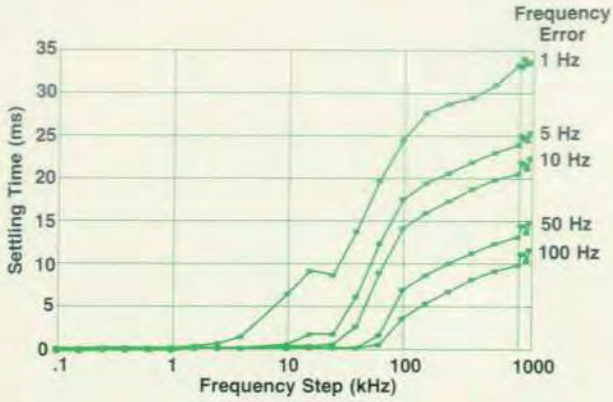


Fig. 2. *Typical settling time as a function of the size of the frequency change and allowable frequency error.*

Fig. 1 shows a discrete sweep with timing signals produced by the HP 3326A. The Z-blank signal occurs at the start of the sweep, and the marker occurs at the end of each timing cycle. The differences in marker pulse width for the first element and for the subsequent elements is caused by software timing. Fig. 2 shows typical settling times for various frequency changes.

Acknowledgments

Discrete sweep was first proposed by Dave Bartle. The idea was encouraged by Max Ramble and supported by Larry Smith.

Michael B. Aken
Development Engineer
Lake Stevens Instrument Division

loop phase stability. Drifts in bias currents translate to drifts in output phase. Drifts in API currents cause temperature dependence in phase ramp cancellation.

Monolithic operational amplifiers are used to implement the loop integrator amplifier and current summer amplifier to reduce complexity and parts count.

Reverse signal path isolation is important, particularly in the connection between the VCO and the counter circuitry, and in the counter-output-to-phase-detector connection. If injected into the VCO or phase detector, many of the counter and control chip signals can cause additional spurious responses.

An ECL flip-flop at the VCO output divides the synthesizer output frequency for a 6-dB improvement in phase noise and spurious perfromance, and reduces local oscillator even-order harmonic content to the output mixers to reduce generation of even-order mixer spurious products. The benefits derived from division of the fractional-N output were viewed as more important than the resulting frequency range restriction.

High-Dynamic-Range Output Circuitry

Mix-down signal sources generate output frequencies by heterodyning the RF from the synthesizer with a fixed frequency. To provide good harmonic distortion and spurious performance, mixing is usually done at very low levels (typically 2 to 10 millivolts) resulting in limited signal-to-noise ratios. Large amplifications are then required to provide output levels in the 10V-peak range. The HP 3326A takes advantage of a high-level active mixer which accepts 100-mV peak-to-peak input levels at the low-level port. Harmonic distortion and spurious products are typically

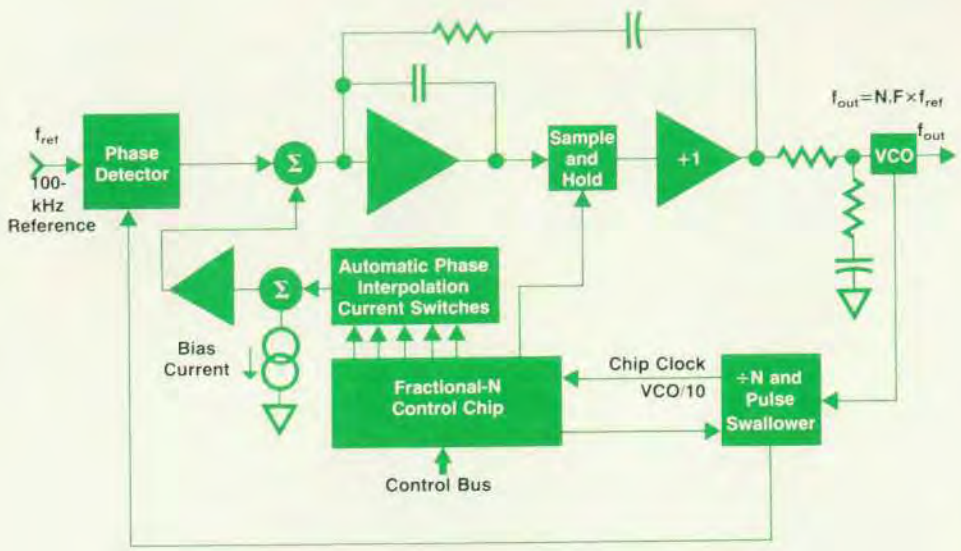


Fig. 5. *Fractional-N synthesizer block diagram.*

below −85 dBc across the 13-MHz band at the output of the mixer (see article, page 25). Active circuits also allow conversion gain, resulting in a mixer output level of approximately 100 millivolts. Subsequent amplification requirements are greatly reduced.

The active output mixer, based on a Gilbert cell multiplier configuration, is implemented with a discrete design to establish control of circuit parameters. Using this approach, even-order spurious mixing responses, which lie in-band for output frequencies greater than 7 MHz, are reduced to imperceptible levels. The active approach also helps maintain an acceptable signal-to-noise ratio.

The RF switches are implemented using current-controlled diode switches with ECL gates as buffer amplifiers. Typical switch isolations of 70 dB are achieved using standard printed circuit layout techniques. To reduce crosstalk and channel isolation further, unused signals in various modes are switched off at the source, again using ECL gate buffers.

Output amplification in the HP 3326A is implemented using high-performance, wideband operational amplifiers in parallel with feed-forward discrete ac amplifiers. Excellent distortion performance at low-frequencies is achieved, with good slew rate performance for higher-frequency rectangular waveforms. Care had to be exercised to tailor the amplifier frequency responses. Overall loop gain has to be high as the ac circuit gain increases to avoid aberrations in phase and amplitude responses of the overall amplifier. Slew rates better than 1300 volts per microsecond are achieved, and distortion is below −80 dBc up to 50 kHz with full scale signal levels of 20 volts peak-to-peak at the output amplifier (10V p-p into 50Ω, 50Ω back-matched voltage source).

Output Attenuation and Signal Combiner

Output attenuation is accomplished with relay-switched pi network pads. Steps of 10, 20, and 40 dB are provided for a total of 70 dB of fixed attenuation. With the 10 dB of high-resolution attenuation from the leveling circuitry, a total attenuation range of 80 dB is achieved.

Relay switches are provided on both attenuator assemblies to transfer signals from the output connector to the calibration circuits. By disconnecting the output signals from the front-panel connector, calibration is accomplished without being affected by user loads. To maintain source termination, the 40-dB pad is switched in during calibration.

The Channel B attenuator contains a switch to transfer Channel B signals from the front-panel connector to the internal modulation circuitry (PM on the main fractional-N circuit and AM on the Channel A level control circuits).

Instrument Controller and Power Supplies

The instrument microcomputer/controller is based on a 68B09 microprocessor. Memory is allocated as follows: 58K of ROM for program storage, 2K of nonvolatile RAM for saved instrument states, 2K of scratchpad RAM for stack space and program use, and 2K of memory mapped I/O for instrument control. The clock rate is 8 MHz. Support circuitry includes a programmable counter/timer to provide the one-millisecond interrupts for front-panel refresh and keyboard read, and a 9914 HP-IB interface chip to handle bus protocol and I/O. Nonvolatile RAM, backed up with a lithium battery, is included to provide nine saved instrument states. An X-drive DAC, also driven by the programmable counter/timer, provides an X-axis output proportional to sweep rate. Marker and Z-blank functions round out the sweep signal set.

Because of the interference generated by high-level logic signals, and the interference conducted as the internal bus picks up other signals in the instrument, the internal instrument bus is pulled low actively whenever the bus is not in use. This provides additional isolation by reducing bus impedance and the pickup of internal electric fields caused by higher-impedance phenomena.

Very clean, linearly regulated power supplies provide +5, +15 and −15 volts to the instrument. A separate +5V isolated supply is used to maintain HP-IB ground isolation. Auxiliary ±30V supplies power the optional high-voltage amplifiers, and an unregulated +18V provides standby power to a separate regulator on the optional reference oven assembly.

The power supplies are implemented using active linear regulation based on operational error amplifiers for low noise and high loop gain. The supply reference voltage is generated from a heavily decoupled, temperature compen-

(continued on page 18)

Two-Channel Synthesizer Phase Calibration

The calibrator of the HP 3326A Two-Channel Synthesizer provides not only the amplitude and offset accuracy enhancements that users have come to expect from Hewlett-Packard, but through the use of phase calibration, it also provides new levels of wideband phase accuracy. The combination of high phase resolution and phase correction techniques allows fast, repeatable programming of in-phase signals or phase offsets up to 720° in 0.01° steps between the output channels.

Fig. 1 shows phase accuracy as a function of frequency in the HP 3326A. The accuracy is limited on the low end by phase noise in the HP 3326A and on the high end by the residual time uncertainty limitations of the calibrator.

Phase calibration accuracy improves with identical waveforms (sine/sine or square/square), higher amplitudes, equal amplitudes, and midrange frequencies. At lower frequencies the results are more susceptible to noise. This noise disturbs the crossover points and makes it more difficult for the phase algorithm to converge. Phase compensation of the modulators and attenuator allows the instrument to calibrate phase in the areas of highest accuracy and then modify the phase for the frequency (attenuator compensation) and amplitude (modulator compensation) that are programmed. Phase matching of all cables, both internal and external, is necessary for high-frequency phase calibration.

The problem of calibrating phase accurately over four decades of frequency and 20 dB of dynamic range is complicated by several considerations. Among these are cable phase match, calibrator channel and offset match, phase null accuracy, indirect phase shifts in attenuators and modulators, ground loops and crosstalk, and noise, harmonic, and/or spurious content on the two waveforms.

The phase calibrator is designed to minimize the errors encountered in phase calibration through both hardware and software techniques. The basic calibrator block diagram is shown in Fig. 2. The technique used for phase comparison is not new, but it is applied here to wideband signals instead of the usual narrowband IF signals. The input switching connects the calibrator input to ground, or connects the Channel A and Channel B signals to measure the phase of Channel A with respect to Channel B, or vice versa. Zero-crossing detectors combine both ac and dc feedback to produce a square wave with hysteresis for both high-frequency and low-frequency input signals. The phase detector is alternately set and reset by the outputs of the zero crossing detectors. Outputs of the phase detector have a dc level that is proportional to the phase difference of the two signals. The low-pass filter/comparator combines differential filtering with a preset detection point to determine when the relative phase passes through 180°. The gain of the comparator allows

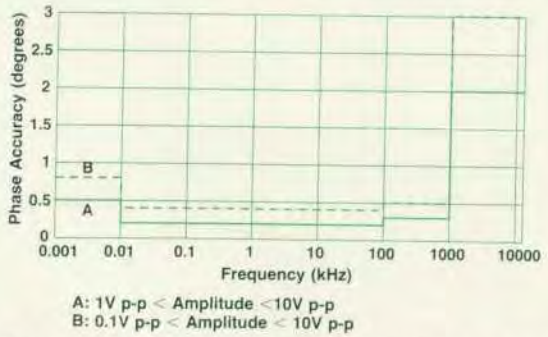


Fig. 1. *HP 3326A Two-Channel Synthesizer phase accuracy specifications.*

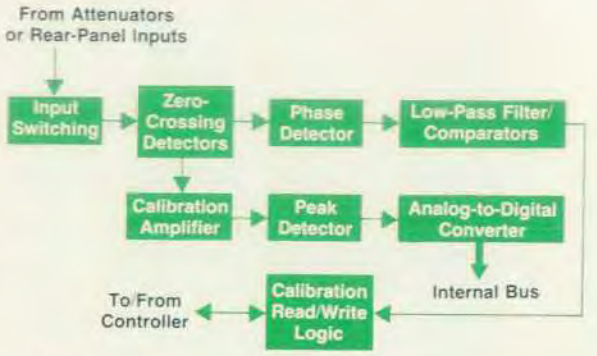


Fig. 2. *Phase calibrator basic block diagram.*

the calibrator to detect phase changes on the order of 0.003°. A comparator state vector signals phase crossover to the internal microprocessor. The HP 3326A firmware controls both the settling time of the filter/comparator and the phase step size. Once the comparator is set to a known value, the phase offset is stepped in smaller and smaller alternating increments until the exact 180° point is known. The signals to the calibrator are then reversed in the switching network and the procedure is repeated. One half of the difference between the two phase offset readings is the calibrated phase relationship. Many of the calibrator phase errors cancel in this procedure.

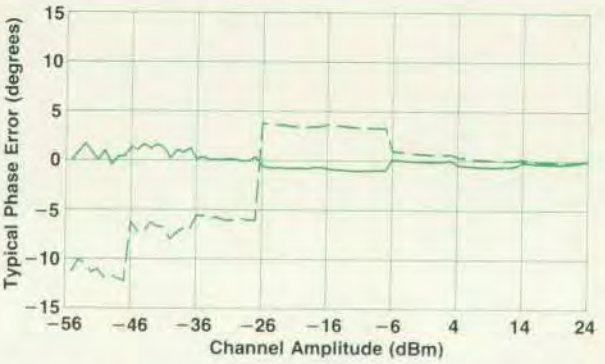


Fig. 3. *HP 3326A attenuator phase shift. Dashed line: uncalibrated. Solid line: corrected.*

Verification of the accuracy of the phase calibration system requires the ability to measure the calibrated outputs of the HP 3326A. This is done with the HP 3577A Network Analyzer and an HP 9000 Series 200 Computer. This testing requires the removal of systematic errors through matched cables and the substitution of a power splitter. Measured errors are cancelled by the controller. Resolution , stability, and accuracy are measured within 0.05°. A counter measures the phase relationships of the square wave so that the optimum values can be maintained in the presence of symmetry errors.

Fig. 3 shows the uncalibrated and corrected phase shifts of the attenuators.

Michael B. Aken
Development Engineer
Lake Stevens Instrument Division

(continued from page 16)
sated Zener diode. Load regulation for the 15V supplies is typically within 10 μV at the sense point for a 2A change in load current. Ripple at 120 Hz is typically no more than 10 μV. Requirements for power supply rejection in the critical circuits, particularly in the synthesizers and low-level portions of the output circuits, are greatly reduced.

Packaging Techniques

Packaging for an instrument with 80 dB of dynamic range presents a considerable challenge. Circuit isolation demands the use of tightly sealed individual circuit compartments for critical analog functional blocks, and for the digital interfaces to the controller. The HP 3326A uses a relatively inexpensive aluminum sand casting. Flash is cleaned from the casting, and the top and bottom surfaces are machined, drilled, and tapped for close seals to the six-layer motherboard and the compartment top covers. Circuits less susceptible to internal EMI, such as the power supply and controller, are packaged on standard printed circuit boards with edge-guide mounting and motherboard connectors. Sensitive RF signals are routed across the top of the cast card nest in double-shielded cables. Ribbon cables route digital signals to the front-panel display and keyboard, and to the rear-panel HP-IB connector.

An additional packaging constraint is imposed by the requirement for dc isolation between the inner chassis and the instrument side frames and outer case. Two separate ground systems are required for the motherboard, and insulators are installed between the card nest and the side frames. Separate grounds maintain HP-IB isolation and reduce multiple signal current return paths, which lead to amplitude errors at low levels (classic attenuator problem).

Acknowledgments

As with most complex design projects, the list of contributors to the success of the project is a long one. Middle project phases were managed by Larry Smith and Paul Thomas. Larry Smith continued as sole manager after the move to Washington as the Lake Stevens Instrument Division of Hewlett-Packard split from the parent Loveland Instrument Division in Colorado. A special note of thanks is extended to Larry for an outstanding job of management.

Lee Gregory and Kurt Rentel were key designers during the initial investigation and definition phases. Andy Cassino contributed to the investigation of design improvements to the fractional-N technique. Steve Reames contributed initial designs for the power supplies and reference frequency circuits. Tim Lock was the original product design engineer.

As design team changes resulting from the divisional move stabilized, a talented project team carried out the design and implementation of the instrument. Dave Bartle, Katie Potter, and Rich Wilson designed the instrument firmware. Al Lesko had responsibility for the fractional-N system until he left to return to school. Bill Ginder completed the fractional-N design. Grant Bower was responsible for power supply and controller circuit designs. Manfred Bartz contributed the output amplification and attenuator designs. Dave Rassmussen designed the modulator, the RF switches, and the output filtering, and contributed to the output mixer design along with Bill Ginder. Curt Allen was responsible for the development of the calibration and square/pulse circuits. Andy Purcell had design responsibility for the AM and offset assemblies, and contributed to instrument evaluation and testing. Paul Gallagher and Ann Testroet were responsible for the package development in its final form. Debbie Fromholzer contributed the industrial design support for the instrument. Clark Nicholson, Joe Diederichs, and Larry Bennet developed the instrument turn-on and test system for manufacturing. It has been our personal pleasure to work with all these people during the course of the project.

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Applications of a Two-Channel Synthesizer

by Michael B. Aken

THE HP 3326A TWO-CHANNEL SYNTHESIZER offers the user exceptional versatility with its combination of two frequency synthesizers, phase calibration, synchronized sweeping, and a frequency agile discrete sweep. A few examples of its applications are:

HP 3326A Feature	Applications
Multiphase Testing	Three-phase control circuit design and testing
Discrete Sweep	Sonar testing
	Two-tone rejection testing
	Dual-tone multifrequency generation
Two-Tone Mode	Communications scrambling
	Illegal tone combination generation
	Tone decoder testing
	Mixer testing
	Intermodulation distortion
Two-Phase Mode	Transducer testing
	Two-tone jitter generation
	Phasemeter testing
	Phase locking

Multiphase Testing

The ability to control and set the relative phases of three or more signals easily is important in the development and testing of control systems that demand flexible phase requirements on the inputs. The HP 3326A can calibrate, equalize, or offset its phase with respect to any number of other HP 3326As in a minimum number of steps. If power splitters are used, the system can be calibrated without removing any cables. For more than two HP 3326As, the user has the choice of either daisy chaining the phase reference or connecting the phase reference from a master instrument to all of the remaining instruments. The daisy chain method introduces a cumulative phase error, while the parallel method decreases the reference amplitude by 6 dB for each additional instrument.

The sources of phase error in multiphase calibration (or in external calibration) are dissimilar waveforms (square or sine), the lack of phase matching of cables used in the system, the amplitude ratio of the two signals used in external calibration, and the absolute amplitude of these signals.

Maximally accurate phase calibration using the external calibration ports requires that both the slew rates (dv/dt) and the harmonic content of the two input signals be closely matched. At frequencies below 1 kHz it is extremely difficult to provide both dc blocking in a 50Ω system and sufficient squaring-circuit hysteresis in the calibrator without affecting higher-frequency phase performance. In multiphase applications below 1 kHz, additional instrumentation is needed to provide calibrated phase performance.

Fig. 1 shows the normal connections for multiphase operation. Fig. 2 shows the additional equipment needed for operation below 1 kHz.

Logic Signal Simulation

At first, the use of a precision two-channel function generator to drive logic circuits may seem like overkill. Closer inspection reveals that the capabilities for providing worst-case analog signals or real simulation of spurious conditions are unmatched. The following are some brief examples of using the HP 3326A to exercise logic circuits:

- The absolute phase calibration between the two square outputs suggests an application for determination of the phase sensitivity of two clock systems to errors in overlap. This feature can also be used to determine setup times in edge-triggered systems.
- Its amplitude resolution and stability along with its dc offset resolution and accuracy suit the HP 3326A for worst-case testing of external TTL-compatible ports for margin requirements.
- The ability to modulate channel A precisely with channel B allows another form of worst-case testing. The use of the built-in combiner allows precise phase jitter of different values and bandwidths to be introduced at a logic input. The phase jitter in degrees peak is the arc tangent of the ratio of the two amplitudes.
- The ability to multiphase calibrate two HP 3326As in pulse or square mode allows generation of either four

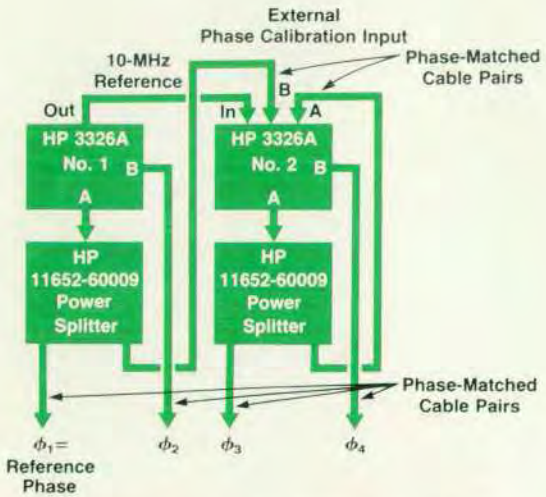

Fig. 1. *The HP 3326A Two-Channel Synthesizer can calibrate its phase with respect to any number of other HP 3326As in a minimum number of steps. The normal connections for such multiphase calibration at frequencies above 1 kHz are shown here for four-phase calibration.*

Measuring Intermodulation Distortion with a Two-Channel Synthesizer

A good example of the capabilities of the HP 3326A Two-Channel Synthesizer is a swept measurement of intermodulation distortion (IMD). Analyzing intermodulation distortion provides insight into the nonlinear characteristics of a circuit or system. Common applications are in audio or communications.

The test stimulus or driving signal is usually a composite of two closely-spaced, high-level sine waves. Fig. 1 shows the spectrum of the signal as reproduced by the circuit under test. Note the resulting distortion products. The distortion products to be measured are offset in frequency from the stimulus signals.

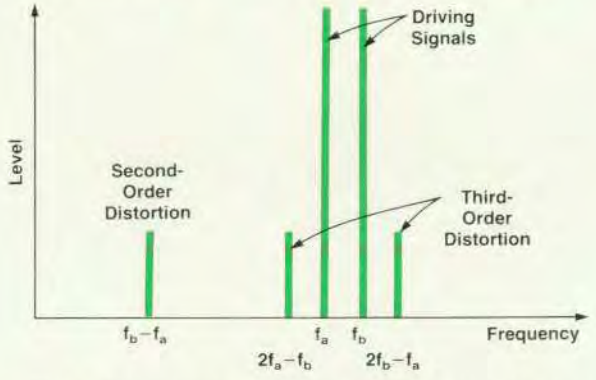

Fig. 1. *Second-order and third-order intermodulation distortion products.*

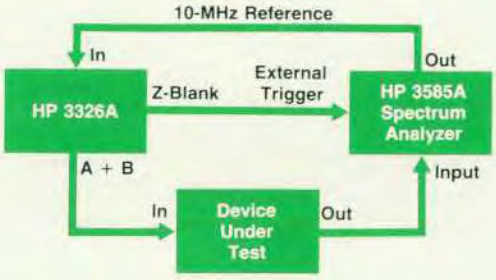

Fig. 2. *Setup for swept intermodulation distortion measurements using the HP 3326A Two-Channel Synthesizer.*

In the past, these measurements were made with two separate sources, an external signal combiner, and a spectrum or wave analyzer to select and measure the desired distortion product.

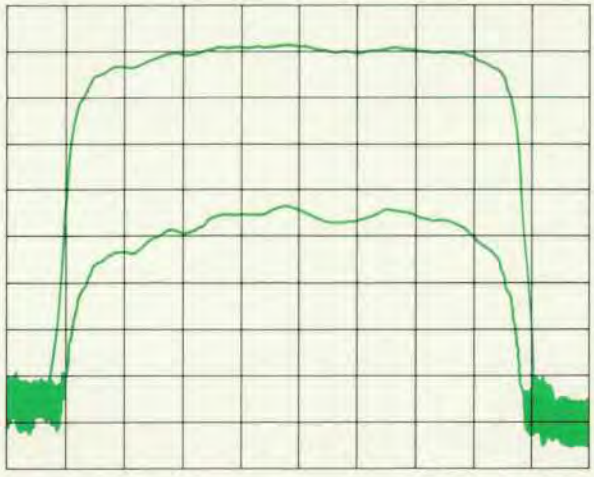

Fig. 3. *Swept third-order distortion measurement of an IF amplifier and filter. Distortion level is the difference between the reference trace (upper) and the measurement trace (lower). Vertical scale: 10 dB/division. Horizontal scale: 5 kHz/division.*

To characterize a circuit over a frequency range of interest, a series of single-frequency measurements were made by successively setting both sources and the analyzer to the appropriate frequencies. Even with programmable instruments under computer control, these measurements were rather slow.

Using the HP 3326A to produce the stimulus signal and the HP 3585A Spectrum Analyzer to measure the response, the measurements are simpler and faster. The HP 3326A has a two-tone mode and an built-in signal combiner to provide a sweeping two-tone signal with IMD as low as −80 dBc.

As shown in Fig. 2, the source and analyzer share a common frequency reference.

The Z-blank signal from the HP 3326A causes the instruments to start their sweeps simultaneously, with the desired frequency offsets. These offsets are maintained while the instruments sweep synchronously to produce a display like that shown in Fig. 3.

Ben Zarlingo
Product Marketing Engineer
Lake Systems Instrument Division

well-defined square waves or two pulse trains.

- Discrete sweep allows a sequence of repeatable square waves or pulses to be used as inputs where repetitive well-known frequencies are required. An example of this is the generation of a pseudorandom set of frequencies to excite a logic system.

The HP 3326A is not limited to square waves in logic testing. Sine waves can be used to test comparators and Schmitt triggers. The HP 3326A can be used to test for amplitude-modulation-to-phase-modulation conversion and hysteresis. Discrete sweep can be used to characterize the delay and response time of comparators.

Communications Testing

The combination of two sources and the ability to calibrate amplitude, phase, and modulation allow the testing and simulation of a large variety of communication devices.

In the world of low-cost instrumentation, the user's expectation for modulation capability of instruments demands that the modulation port be available, and that some nominal full-scale input sensitivity and bandwidth be specified. The HP 3326A, with its calibrated amplitude and phase modulation, offers modulation functions whose specifications are exceeded only by extremely expensive test equipment. Not only is the accuracy exceptional, but the resolution, frequency flexibility, and remote control capability of modulation in the HP 3326A make this instru-

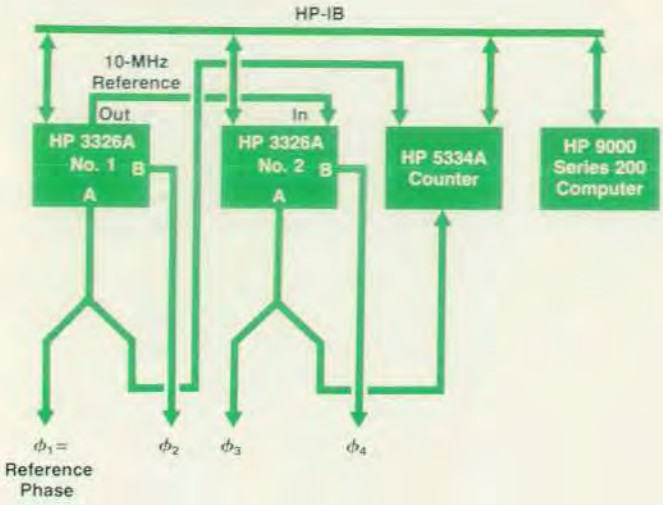

Fig. 2. *Connections for four-phase calibration below 1 kHz, showing the additional equipment needed.*

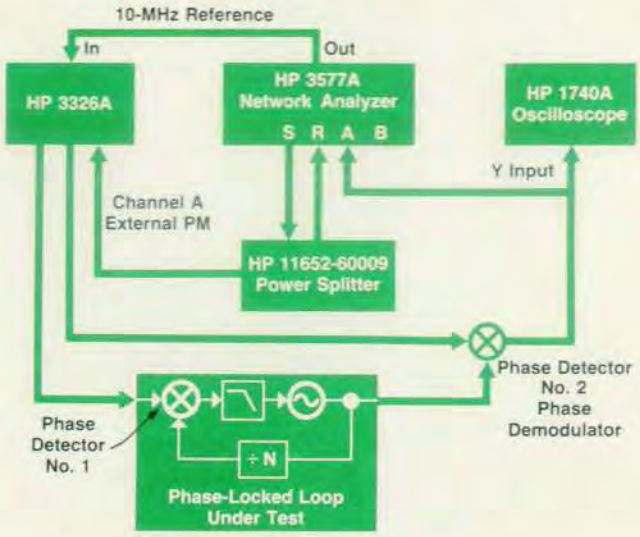

Fig. 3. *HP 3326A simplifies the testing of phase-locked loops and control loops. Shown here is a setup for frequency and phase response measurements.*

ment stand out in high-quality systems applications.

The combiner provides the stimulus for intermodulation tests, and when one or both channels are sweeping , it also provides unequaled ability to look at real-time intermodulation distortion products (see box, page 20). For phase jitter testing through the use of two tones, the HP 3326A can provide calibrated sine waves with a known amount of phase jitter. In this case (two combined tones) the signal also contains a modulation component, unlike the constant amplitude of the phase modulated signal.

The combination of linked sweep, phase calibration, and various output functions can allow previously unavailable mixer and phase detector testing in noncontroller environments. When both channel synthesizers are sweeping in the same direction, phase repeatability and single-point accuracy are maintained. Standard sweep with marker is available for conventional filter testing. Discrete sweep allows real-time settling-time measurements of filters.

Control Loop Testing

Although applications in testing of control loops and phase-locked loops have existed a long time, the HP 3326A brings simplicity of operation to these measurements. This is because the HP 3326A can generate two different outputs whose phase can be calibrated and offset. Referring to Fig. 3, this allows the demodulator #2 signal to be generated and set up with a mininum of effort. The use of the HP 3577A Network Analyzer[1] as a detector allows both the amplitude and the phase of the loop to be measured.

Reference

1. R.A. Witte and J.W. Daniels, "An Advanced 5-Hz-to-200-MHz Network Analyzer," *Hewlett-Packard Journal*, Vol. 35, no. 11, November 1984.

Synthesizer Firmware for User Interface and Instrument Control

by David A. Bartle and Katherine F. Potter

INSTRUMENT FIRMWARE (software in read-only memory) performs three major functions in the HP 3326A Two-Channel Synthesizer. First, it implements the user interface presented by the front panel and the HP-IB (IEEE 488) remote control bus. Second, it provides all of the control algorithms and signals for the internal circuitry. Third, it enhances the instrument's performance with extensive self-calibration and self-test capabilities.

Running this firmware is a 68B09 8-bit microprocessor with 64K of address space apportioned as follows: 58K in ROM, 4K in RAM (including 2K of nonvolatile RAM), and 2K for I/O. The primary language used for the firmware is Pascal adapted for use in an instrument control environment. Approximately 92% of the firmware (11,475 lines of

source code) is written in Pascal and the remaining 8% is written in assembly language.

Design Philosophy

The most important objective for development of the firmware was to implement a friendly and reliable user interface at the front panel and the interface bus (HP-IB). Second, during the product development, it was crucial to support the hardware development effort with firmware for control of individual circuit boards, system integration, and testing. Third, completing the firmware in a timely fashion with no known errors (bugs) was important.

The firmware design task was broken into a sequence of design steps, using the concepts of structured software design.[1] The initial task was the generation of a document detailing the proposed instrument feature set and operation from a user's point of view. This document was used as a design guide for the firmware development. It clarified the instrument's proposed operation to everyone involved in the instrument development effort. This document was carefully maintained to ensure an accurate, current picture of the intended instrument operation.

Next, a software architecture was proposed and expressed graphically as a hierarchy chart.[2] The modules in the hierarchy chart were defined by their logical function and data use. Architecture walkthroughs were conducted to refine the architecture and to ensure that it fit the needs of the definition.

With the architecture designed, the internal structures of individual modules in the hierarchy were defined and designed in a top-down order: the highest-level module was designed first, then the next-highest-level module, and so on. Each module was further decomposed into procedures (and/or functions) supporting the defined function of the module. The internal logic of each procedure was designed using the pseudocode technique.[3] Complete modules were subjected to a design review.

Finally, Pascal source code was generated for the procedures contained in each module, again in a top-down order. If possible, modules were individually tested as the source code generation was completed. Module integration and testing began with the completion of the core of the architecture, which included the EXECUTIVE, KEY, HP-IB, COMMAND BUILDER, DISPLAY, and EXECUTE modules (see firmware block diagram, Fig. 1). Other modules were initially implemented as dummy or do-nothing modules.

Firmware testing was performed both manually and by software designed for testing the HP 3326A firmware.[4] This software package is written in BASIC and runs on an HP Series 200 Computer, which controls the HP 3326A via the HP-IB. It is designed to test the entire user interface as well as parameter limits, command syntax, error conditions, and bus reliability.

Compiler

In addition to a viable design philosophy and plan for a large firmware development effort, it is important to have appropriate tools to support the design effort. A Pascal compiler was developed for the 68B09 microprocessor. This compiler runs on an HP 9000 Series 200 Computer. Several special compiler features are included to expedite the development task. Compilation of individual modules allows designers to work in parallel and reduces compiler overhead time. Floating-point math capability simplifies amplitude control and calibration algorithms. Binary-coded decimal (BCD) math supports the necessary dynamic range for frequency entry and control (1 microhertz to 13 MHz is 14 decades). A first in, first out (FIFO) buffer data structure, referred to as the message queue, allows easier implementation of communication between the EXECUTIVE, the real-time processes, and various modules.

Design Implementation

The main program, the EXECUTIVE, is responsible for initializing the instrument at power-on, processing inputs and events from other processes, responding to programming errors, checking the hardware fault register for hardware errors, and ensuring orderly state changes in the hardware.

The INITIALIZE module is used by the EXECUTIVE to perform all power-on hardware and software initialization and to set up the instrument state (frequency, amplitudes, etc.). After programming the initial instrument state, INITIALIZE performs a self-test and an instrument calibration.

The remaining portion of the EXECUTIVE is a loop which checks through an ordered list of potential activities for the one that has requested processing. This ordering causes each input to be completely processed before the next input

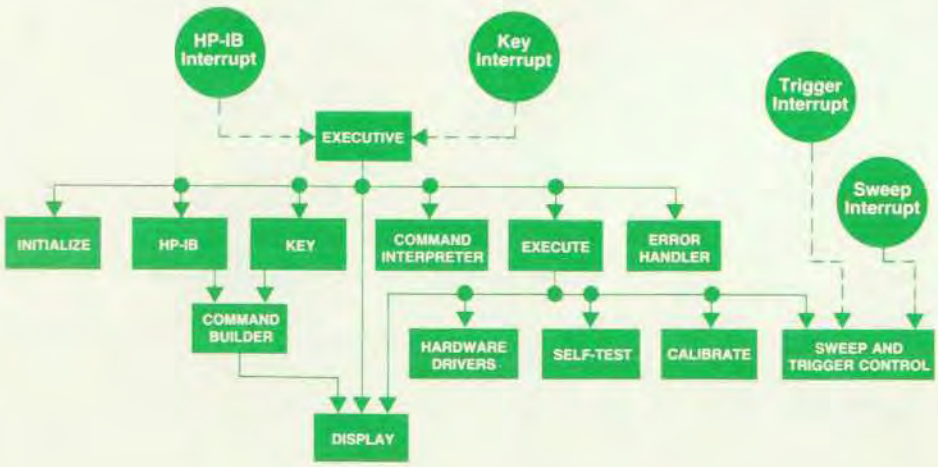

Fig. 1. *Firmware architecture of the HP 3326A Two-Channel Synthesizer.*

is handled.

Several interrupt processes interact with the EXECUTIVE. These are the HP-IB input process, the keyboard input process, and indirectly, the sweep process and the external trigger process. The communication between each of these and the EXECUTIVE is controlled by a special buffer, called a message queue. These queues provide synchronized exchange of data between interrupt modules and the EXECUTIVE to prevent interaction problems.

When a key is pressed or an HP-IB character is sent, the input is placed in a message queue. The EXECUTIVE recognizes the input and sends it, with the necessary input history, to the KEY or HP-IB module. These modules use the BUILD COMMAND module to return the updated input history and a complete or partial command. An entry state machine keeps track of the status of the input process.

When a complete command is generated, the EXECUTIVE sends it to the COMMAND INTERPRETER where the command is checked for programming errors. If there are no errors, a list of tasks used to implement the command is placed in a task message queue. Otherwise, an error is reported. When the EXECUTIVE finds a task in the task message queue, it calls on EXECUTE to perform that task.

If there is an error, the EXECUTIVE sends it to the ERROR HANDLER, which reports the error via the HP-IB status register and/or displays it and starts an error timer. When the timeout occurs, the ERROR HANDLER is called again by the EXECUTIVE to replace the error message with the previous display.

Calibration Firmware

HP 3326A performance is enhanced by extensive self-calibration. The output signal dc offset, amplitude, and phase are measured close to the output connectors. These measurements are used by the calibration firmware to modify the algorithms controlling those parameters to improve their accuracy. The HP 3326A calibrates signal amplitude, dc offset, phase, internal amplitude modulation, and internal phase modulation. Undesirable phase shift caused by level control circuitry and attenuators is also compensated. Altogether, the HP 3326A uses 24 calibration correction factors.

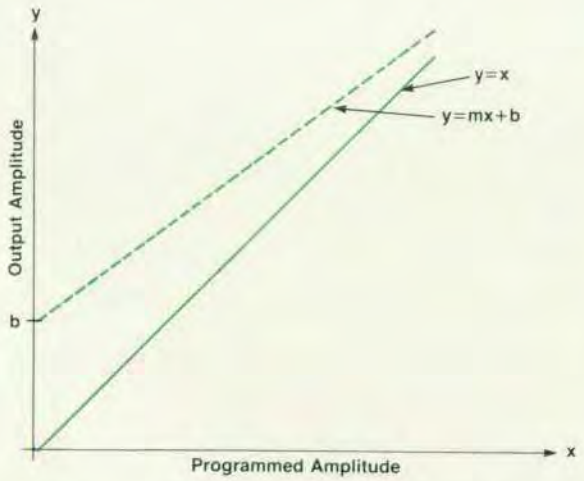

Fig. 2. *For an ideal amplitude control system, the output amplitude equals the programmed amplitude (solid line). For a real system, the response (dashed line) differs from the ideal. The HP 3326A firmware measures two points on the actual response curve, computes the slope and intercept, and corrects for system errors.*

Amplitude Calibration

The amplitude control for the HP 3326A consists of a DAC-controlled dc signal modulating the level of a 20-MHz signal. This gives a 10-dB range of amplitude control with 0.01-dB resolution. Fixed attenuation of up to 70 dB can be programmed by combining 10, 20, and 40-dB pads.

For an ideal amplitude control system, the output amplitude equals the programmed output amplitude, as shown by the solid line in Fig. 2. For an actual system, gain and loss variations, DAC offset, gain errors, and other factors yield an amplitude response described by the dashed curve in Fig. 2. The calibration firmware measures the actual response and corrects the input to the DAC (digital-to-analog converter) so that the actual response is mapped more closely into an ideal response. Two points on the actual response (dashed line in Fig. 2) are measured and used to compute the slope m and the Y-axis intercept b. These are used to compute corrections for any programmed amplitude.

The HP 3326A calibrates the peak amplitude of each channel for the sine and square functions. This includes computation of slope and offset corrections for each function, for a total of four calibration correction factors for each channel.

DC Offset Calibration

The dc offset of each channel is calibrated by computing a gain error correcton for each channel. Unlike ac amplitude calibration, there is only one dc gain correction to be computed for each channel because there is only one signal path from the dc control circuitry to the output. However, the ac signal paths contribute unwanted dc offsets that must be compensated by the dc control circuitry, and therefore several offset correction values are computed, for a total of six dc offset calibration correction factors per channel.

Phase Calibration

The HP 3326A performs three types of phase calibration: internal, external, and multiphase. Internal phase calibration calibrates the phase of Channel B with respect to Channel A at the output connectors on the front panel. External phase calibration calibrates the phase of Channel B with respect to Channel A at the external calibration connectors on the rear panel. Multiphase calibration calibrates the phase of Channel A with respect to another HP 3326A reference signal at the external phase calibration connectors on the rear panel.

Internal Amplitude Modulation Calibration

Internal AM (Channel B modulating Channel A) is calibrated by measuring the peak of the modulation envelope and comparing it to the expected value. A calibration correction factor, which is the ratio of the expected value to the measured value, is then applied to the programmed amplitude of the modulating signal, Channel B.

Internal Phase Modulation Calibration

A phase modulation constant in degrees per volt is calculated for Channel A by measuring its phase shift when a dc phase modulation reference is applied. This constant is then used in programming the amplitude of Channel B when it is used as the internal phase modulation source for Channel A.

Modulator Phase Correction

The sine modulator exhibits a side effect of a phase change when the modulator level is changed. The phase shift of each modulator is measured at 10 dB below full scale. This measured phase shift is used as an end point of a predetermined modulator phase-versus-level response curve. The phase error at various modulator levels is corrected by applying an opposing phase shift whose magnitude is determined from this curve. The modulator phase shift is corrected as amplitude is changed. No attempt is made to compensate for the square modulator.

Attenuator Phase Shift Correction

The attenuators used for level control exhibit a fairly linear phase shift as a function of frequency. Compensation for this phase error is achieved by applying an opposing phase shift whose magnitude is determined by linearly interpolating average attenuator phase shift values measured at 13 MHz. A value is permanently stored for each range (0 to 70 dB of attenuation). Each value represents the combination of one or more attenuators. Whenever an attenuator is changed for either channel or a phase calibration is performed, a new phase correction value is computed and applied to Channel B. This correction is only applied in the two-phase and pulse modes.

Sweep Control Firmware

The sweep control firmware is responsible for starting, controlling, and stopping sweeps, for generating markers, Z-blank and X-drive outputs, and for responding to external triggers. Once the sweep has started, the firmware is interrupt-driven. The sweep firmware can write commands to both of the HP 3326A's fractional-N frequency synthesizers simultaneously to provide synchronous sweep starts and to increase discrete sweep dwell time accuracy.

Sweep programming is table-driven. When the sweep is reset, all the critical internal frequencies (start, stop, rate, and markers) are calculated for both the sweep and the retrace. These values are placed in a table indexed by the sweep state. The main fractional-N synthesizer generates an interrupt at each critical frequency to reactivate the sweep process. At each such interrupt, the sweep state machine reprograms the fractional-N frequency synthesizers with values from the table and advances to the next state.

Each sweep type—ramp, triangle, and discrete—has a different state machine. Ramp sweep, for example, cycles through the following states: sweep from start to marker, sweep from marker to stop, retrace from stop to start. If there is no marker, then ramp sweep alternates between sweep from start to stop and retrace from stop to start.

Synchronous sweep start of both the Channel A and Channel B outputs is possible with a combination of hardware and firmware. The hardware provides the capability to send instructions to both fractional-N synthesizers simultaneously. To start the sweep synchronously, the firmware enables this synchronous loading, preloads the start sweep instruction, and at the appropriate time, loads the instruction to both channels. Because both synthesizers are operating with the same reference clock, their responses are synchronous.

The discrete sweep firmware also takes advantage of synchronous loading. After programming each frequency step, the firmware prepares for the next step by preloading the Channel A and Channel B frequency values. Then the synchronous instruction loading is enabled and the frequency-to-output instruction is preloaded. When the dwell time has passed, the frequency-to-output instruction is immediately executed by both the Channel A and Channel B fractional-N frequency synthesizers. This overlapping of programming and simultaneous frequency changing allows the duration of discrete sweep elements to be very close to the user-programmed dwell time.

HP-IB Operation

The HP 3326A has two different modes of HP-IB data transfer, buffered and nonbuffered. In the buffered mode, each character transferred over the bus is placed in a buffer, and another character can be transferred immediately. Control is not returned to the EXECUTIVE until the buffer is full or no more data transfer is attempted by the controller. In the nonbuffered mode, after each character is transferred, control is returned to the EXECUTIVE and further processing may occur. The buffered transfer has the advantage of minimizing the data transfer time between a controller and the HP 3326A; this is useful if several instruments are being controlled simultaneously, as in an automatic test system environment.

Acknowledgments

Larry Smith provided the leadership to get the firmware development organized and under way. Ken Snyder was responsible for the 68B09 compiler and assembler development and support. Rich Wilson contributed many good ideas to the overall software architecture and implementation, as well as writing the HP-IB, EXECUTE, and SELF-TEST modules. Many thanks to Andy Purcell for his contributions to the development of the firmware test software and to Linda McGee who contributed many hours of firmware testing.

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2. M.L. Gembarowski, "Software Methodology Preserves Consistency and Creativity," *Hewlett-Packard Journal*, Vol. 36, no. 3, March 1985.
3. R.S. Pressman, *Software Engineering: A Practitioner's Approach*, McGraw-Hill, 1982.
4. G.J. Meyers, *Software Reliability*, Wiley-Interscience, 1976.

A High-Level Active Mixer

by William M. Spaulding

TO PROVIDE LOW-BAND COVERAGE, most synthesized signal sources require the use of an output mixer to heterodyne RF signals down to baseband. The HP 3326A Two-Channel Synthesizer accomplishes this mixing function with a high-level, active mixer design based on a standard Gilbert cell configuration.[1]

Mixer designs based on the Gilbert cell configuration shown in Fig. 1 have been used for many years in both discrete and monolithic forms. Like diode mixers, these circuits have performance limitations, particularly in the area of balance. Active approaches also introduce excess noise, primarily because of base circuit resistances.[2,3] However, when noise considerations are treated appropriately, active designs have some very distinct advantages.

One advantage is conversion gain. Mixers distribute the input power among several frequencies. As a result, the level of the desired sideband (usually the lower sideband in a source) is 7 to 10 dB below the RF input port level; this is conversion loss. Active devices amplify these signals during the mixing process. Conversion gain in an active mixer is limited by the impedance levels (noise and filtering constraints) at the collectors of the output transistors, and by the amount of local feedback used for linearization of the low-level differential pair. Gains of 0 dB are readily achieved, resulting in an overall sideband level improvement of as much as 16 dB over a diode mixer.

Another advantage of active designs is that LO port levels can be lower than those in a diode mixer. Active bipolar differential pairs can be fully switched with signal levels of approximately 100 millivolts peak-to-peak across the input.[4] This corresponds to a level of approximately −10 dBm. Even if the bases are overdriven by 6 dB, LO amplification requirements are eased by as much as 20 dB. For a fixed port balance, feedthrough of LO power to the output is similarly reduced.

A third advantage is that active mixers isolate reflected power, which is always a problem in diode mixers. With a current-source-driven resistive structure at the IF port of an active mixer, the source match can be very good. The filter reflections are terminated in these resistors, and little energy is reflected back into the active devices or into the filter to be rereflected.

For these reasons, and because the frequency scheme of the HP 3326A Two-Channel Synthesizer is well-suited to an active approach, an active mixer was selected for the instrument.

Theoretical Considerations

In the generalized Gilbert cell multiplier shown in Fig. 1, mixing action results from periodically reversing the currents in the output collectors by switching the cross-coupled differential pairs at the LO rate, so the RF signal is multiplied by ±1 at the LO rate. Fig. 2 shows a circuit diagram and a simplified representation of a doubly balanced diode mixer. The action of the LO-driven diodes is an alternate connection of ground (from the center tap of the LO transformer) to opposite ends of the RF transformer T2. Current in the RF transformer is reversed at the LO rate, and the RF signal is multiplied by ±1.[5,6]

In the idealized case for either mixer, for a perfect LO square wave and no dc offset on the RF signal, the following mathematical analysis applies. For an LO square wave of unity amplitude and no dc offset:

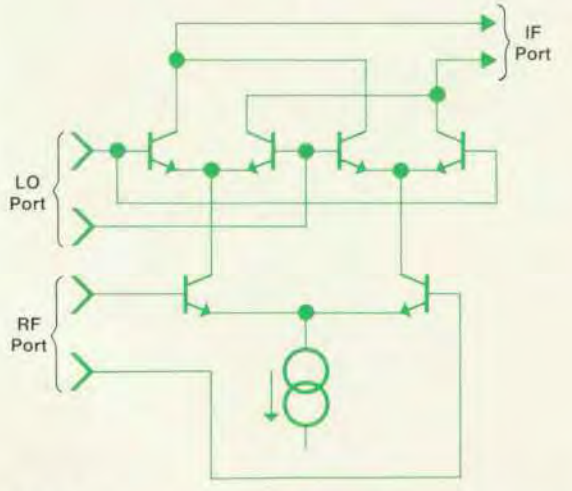

Fig. 1. *Basic Gilbert cell multiplier. Bias networks are not shown.*

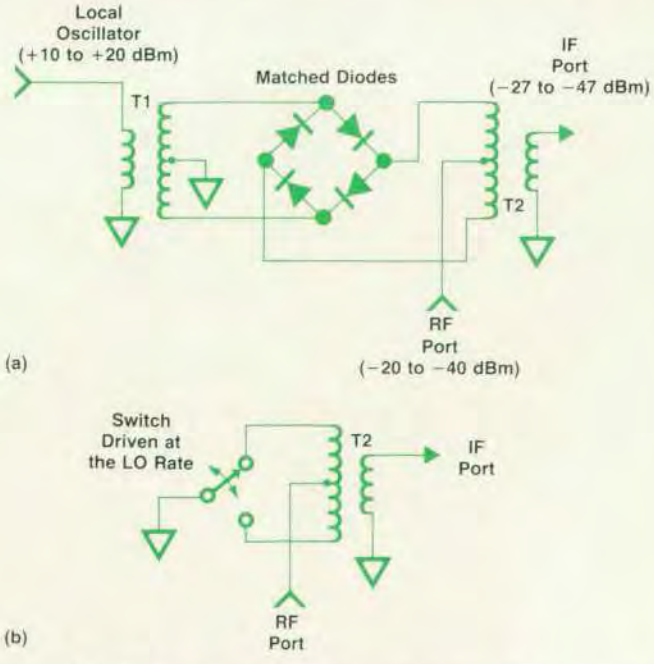

Fig. 2. *The classic diode ring mixer (a) and its equivalent circuit (b).*

$$f_{LO}(t) = \sum_{n=-\infty}^{\infty} \frac{2j}{n\pi} \sin^2(n\pi/2)\, e^{\,j2\pi n f_{LO} t} \qquad (1)$$

Noting that the function is odd (time axis asymmetry) and that the dc term is zero:

$$f_{LO}(t) = \sum_{n=1}^{\infty} \frac{4}{n\pi} \sin n\omega_{LO} t, \quad n \text{ odd} \qquad (2)$$
$$= 0, \quad n \text{ even}$$

Multiplying by a sinusoidal function of amplitude A_{RF},

$$f_{IF}(t) = \sum_{n=1}^{\infty} \frac{4A_{RF}}{n\pi} \sin n\omega_{LO} t \cos \omega_{RF} t, \quad n \text{ odd} \qquad (3)$$
$$= 0, \quad n \text{ even}$$

Since $\sin x \cos y = \frac{1}{2}[\sin(x+y) + \sin(x-y)]$,

$$f_{IF}(t) = \sum_{n=1}^{\infty} \frac{2A_{RF}}{n\pi} [\sin(n\omega_{LO} + \omega_{RF})t + \sin(n\omega_{LO} - \omega_{RF})t], \quad n \text{ odd} \qquad (4)$$
$$= 0, \quad n \text{ even}$$

Equation 4 is the time function for the mixer IF output. Two observations can be made from this equation. First, the IF signal contains no components at the LO or RF frequencies or their harmonics for the idealized case. These signals have been balanced out. Second, the frequency spectrum consists of sum and difference products distributed symmetrically about the LO frequency and its harmonics (Fig. 3).

Now suppose that, as is usually the case in real mixers, the LO square wave is slightly asymmetrical and can be represented as the sum of the pulse and square waves shown in Fig. 4. For small asymmetry, the Fourier series for the pulse waveform is:

$$f_p(t) \approx -\frac{2\tau}{T} - \sum_{n=1}^{N} \frac{4\tau}{T}\left[\cos n\omega_{LO} t + \frac{n\pi\tau}{T} \sin n\omega_{LO} t\right], \qquad (5)$$
$$\frac{N\pi\tau}{T} << 1$$

For N harmonics, the modified LO function is the linear sum of equations 1 and 5:

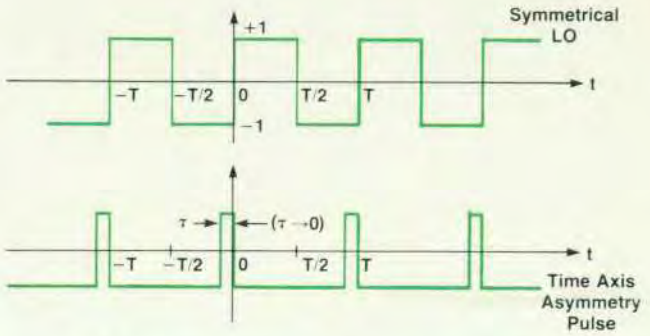

Fig. 4. *An asymmetrical LO waveform can be represented as the sum of the square wave and pulse train shown here.*

$$f_{LO}(t) \approx -\frac{2\tau}{T} + \sum_{n=1}^{N}\left[\left(\frac{4}{n\pi}\right)\left(\sin^2\left(\frac{n\pi}{2}\right) - \left(\frac{n\pi\tau}{T}\right)^2\right)\sin n\omega_{LO} t - \frac{4\tau}{T}\cos n\omega_{LO} t\right] \qquad (6)$$

At the IF port:

$$f_{IF}(t) \approx -\frac{2\tau A_{RF}}{T}\cos n\omega_{LO} t + \sum_{n=1}^{N}\left[\frac{2A_{RF}}{n\pi}\left(\sin^2\left(\frac{n\pi}{2}\right) - \left(\frac{n\pi\tau}{T}\right)^2\right)\{\sin(n\omega_{LO} + \omega_{RF})t + \sin(n\omega_{LO} - \omega_{RF})t\} - \frac{2\tau A_{RF}}{T}\{\cos(n\omega_{LO} + \omega_{RF})t + \cos(n\omega_{LO} - \omega_{RF})t\}\right] \qquad (7)$$

Considering the odd terms from the series:

$$f_{IF}(t)\Big|_{n\,\text{odd}} \approx \sum_{n=1}^{N}\left[\frac{2A_{RF}}{n\pi}\left(1 - \left(\frac{n\pi\tau}{T}\right)^2\right)\{\sin(n\omega_{LO} + \omega_{RF})t + \sin(n\omega_{LO} - \omega_{RF})t\} - \frac{2\tau A_{RF}}{T}\{\cos(n\omega_{LO} + \omega_{RF})t + \cos(n\omega_{LO} - \omega_{RF})t\}\right] \qquad (8)$$

Combining quadrature terms and dropping negligible terms since $n\pi\tau/T << 1$:

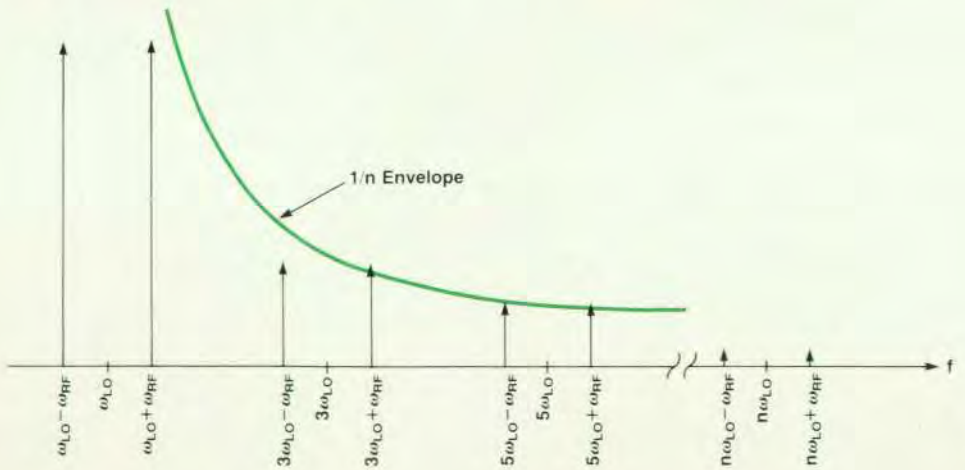

Fig. 3. *Spectrum of the mixer IF signal in the ideal case (linear scales).*

$$f_{IF}(t)\Big|_{n\,odd} \approx \sum_{n=1}^{N} \left[\frac{2A_{RF}}{n\pi}\sqrt{1+\left(\frac{n\pi\tau}{T}\right)^2}\left\{\sin\left[(n\omega_{LO}+\omega_{RF})t+\theta_n\right] + \sin\left[(n\omega_{LO}-\omega_{RF})t+\theta_n\right]\right\}\right] \quad (9)$$

where:

$$\theta_n \approx \tan^{-1}\frac{n\pi\tau}{T} \text{ for } \frac{n\pi\tau}{T} << 1 \quad (10)$$

Recombining all terms (with even terms from the pulse series):

$$\begin{aligned} f_{IF}(t) \approx & -\frac{2\tau A_{RF}}{T}\cos\omega_{RF}t \\ & + \sum_{\substack{n=1,\\ n\,odd}}^{N}\left[\frac{2A_{RF}}{n\pi}\sqrt{1+\left(\frac{n\pi\tau}{T}\right)^2}\left\{\sin\left[(n\omega_{LO}+\omega_{RF})t+\theta_n\right] + \sin\left[(n\omega_{LO}-\omega_{RF})t+\theta_n\right]\right\}\right] \\ & - \sum_{\substack{n=2,\\ n\,even}}^{N}\frac{2\tau A_{RF}}{T}\left\{\cos(n\omega_{LO}+\omega_{RF})t + \cos(n\omega_{LO}-\omega_{RF})t\right\} \end{aligned} \quad (11)$$

Three results are of interest:

1. RF signal feedthrough appears in the mixer output. The RF signal is transferred to the output attenuated by the factor $2\tau/T$.
2. The phase and amplitude of the odd product terms are modified. This is a particularly critical factor in an instrument in which the phase of the IF signal is important, such as the HP 3326A or a vector analyzer. Local oscillator symmetry is critical to maintaining performance even in ideal mixers. When the LO signal is swept over a range of frequencies (as in a source or swept analyzer), variations in asymmetry can cause ripple in the IF signal phase and amplitude response. Asymmetry in fixed LO applications results in an error that can be calibrated out of the system.
3. Quadrature sum and difference products appear around even-order LO harmonic frequencies, attenuated by the factor $2\tau/T$. For many applications, the only importance of the additional product terms is their modification of the desired sideband, or the additional filter requirements imposed to remove them.

Another complication in real mixers is that the RF signal usually has a dc offset. This corresponds to transistor base-emitter offset voltage for an active mixer. In the diode mixer, dc offset can result from either diode mismatch or from the output of a dc-coupled amplifier on the RF port. Such dc-coupled ports are often used in instruments that upconvert from baseband because of the physical size limitations of coupling capacitors, and because of transient settling times associated with large coupling capacitors.

The RF signal can be represented by:

$$f_{RF}(t) = V_{dc} + A_{RF}\cos\omega_{RF}t \quad (12)$$

Multiplying by equation 2 and simplifying:

$$\begin{aligned} f_{IF}(t) = & \frac{4V_{dc}}{n\pi}\sum_{\substack{n=1,\\ n\,odd}}^{\infty}\sin n\omega_{LO}t \\ & + \frac{2A_{RF}}{n\pi}\sum_{\substack{n=1,\\ n\,odd}}^{\infty}\left[\sin(n\omega_{LO}+\omega_{RF})t + \sin(n\omega_{LO}-\omega_{RF})t\right] \end{aligned} \quad (13)$$

Thus, when the RF signal has dc offset, LO feedthrough terms appear in the mixer output signal. The magnitude of the feedthrough terms can easily be (and often is) larger than the desired sideband term.

As a result of these considerations, careful attention to LO symmetry and to residual dc offsets is required in any high-performance mixer design.

Practical Design Considerations for the Active Mixer

Generation of typical source output levels (+25 to +27 dBm) using a diode ring mixer requires a great deal of amplification between the mixer, running with an IF level on the order of −20 to −40 dBm, and the output attenuator. With as much as 60 dB of gain, signal-to-noise ratios at the output become severely degraded unless extreme care is used to design amplification with very low noise figures. When mixing frequencies lie well below the cutoff frequencies (f_T) of the devices, well-designed active mixers can help ease output circuit gain requirements.

Drive configuration. Referring to Fig. 1, there are two obvious choices for driving the LO and RF ports of the active mixer. Single-ended drive could be used by (ac) grounding one side of the respective differential pairs and connecting the other to the signal. Balanced drive generally requires additional circuitry (i.e., transformers or differential amplifiers).

If single-ended signals are used, a voltage approximately equal to half the input level appears at the emitter junctions. Finite and nonlinear current source output impedances result in potentially large and harmonic-rich common mode signals. It has been our experience that any extra circuitry required for balanced drive pays for itself by keeping these emitter points at virtual ground, thereby minimizing common mode signal generation.

Gain control and linearization. Parameter match in active

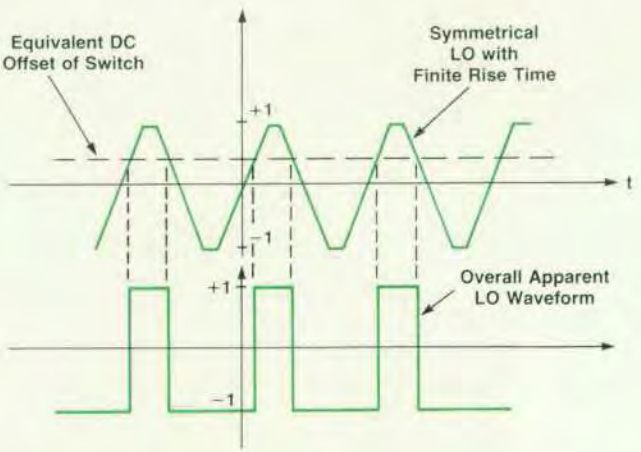

Fig. 5. *Effects of LO rise time and system offset on apparent LO symmetry.*

devices is always less than perfect. The use of local feedback in the form of emitter degeneration in the RF pair accomplishes both linearization of the devices and, once IF port collector impedances have been selected, provides control of overall conversion gain.

Any harmonic distortion generated by the RF pair is translated directly to harmonic distortion in the IF signal. Linearization of the RF pair is extremely important in the HP 3326A Two-Channel Synthesizer because of its specification of −80 dBc for harmonic distortion through audio frequencies.

Estimation of distortion levels. A practical approach to estimation of distortion levels has been developed over the years. The technique is based on peak variations in the value of r_e of the transistor. It is based on the familiar equation:

$$r_e \approx \frac{26}{I_E} \text{ for } I_E \text{ in milliamperes.}$$

For a bias current level of 10 mA, there is approximately 2.6Ω of dynamic emitter resistance. Assuming that the maximum signal current of one milliampere peak is used, the variation of r_e is:

$$\Delta r_e \approx \frac{26}{9} - \frac{26}{11} \approx 0.5\Omega$$

Each side of the differential pair experiences an excursion of 0.5Ω under signal conditions (one side goes up 0.25Ω, and one goes down 0.25Ω). Assume that the devices that make up the differential pair are matched within 1%, that is, the maximum difference in the resistance variation between devices ($\Delta r_e'$) is 0.005Ω. The change in total resistance in the emitter circuit under signal conditions is, therefore, 0.005Ω. The distortion can be estimated as follows:

$$|D| = 20 \log \frac{\Delta r_e'}{R_E}$$

where R_E is the total emitter resistance.

If a value for R_E of 100Ω is used, one might expect to see distortion products at approximately −86 dBc. No insight is provided as to the distribution of the harmonic energy. Although this method probably does not satisfy the purist, we have found it to be a reasonably effective predictor for small nonlinearities.

Common mode suppression and overall balance. Try as one might to avoid them, common mode currents seem to show up in every design. Common mode products would be of no concern except for mechanisms that perform common-mode-to-differential conversions. These conversion mechanisms are usually highly nonlinear, resulting in reinsertion of harmonic energy. Several measures can be in-

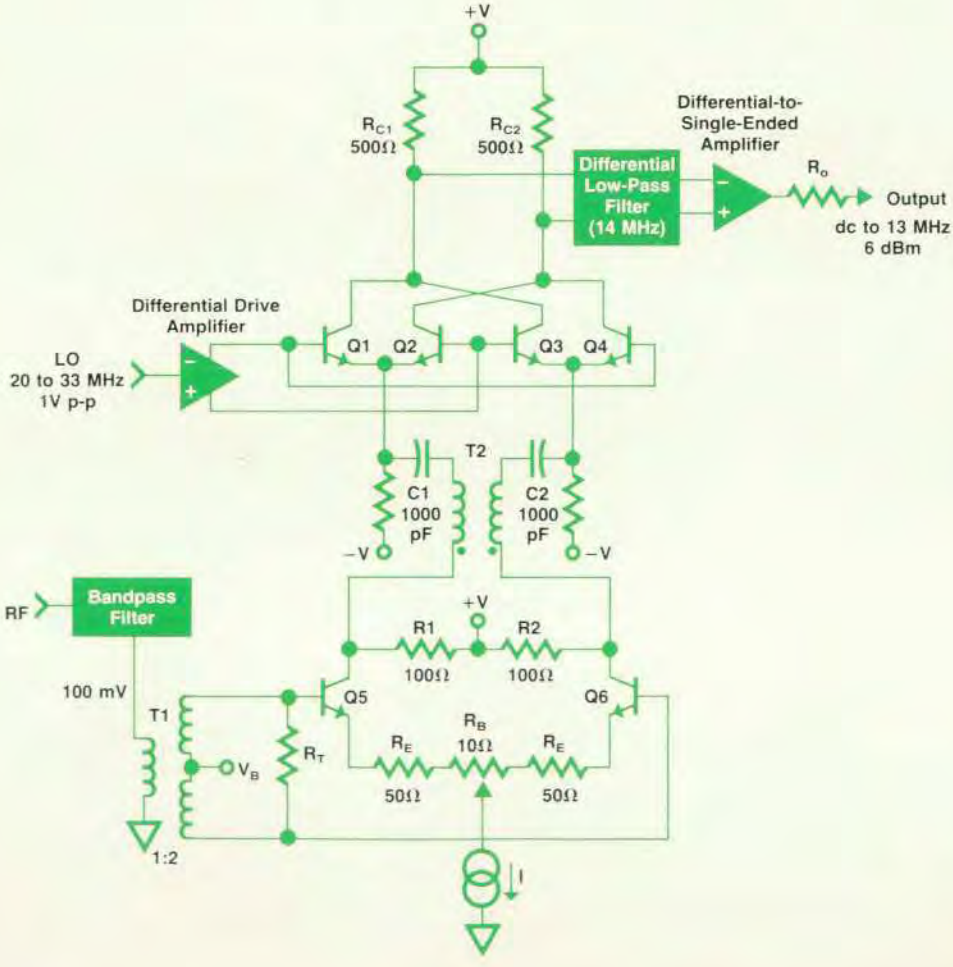

Fig. 6. *Simplified schematic diagram of the active mixer in the HP 3326A Two-Channel Synthesizer.*

voked to reduce the effect of common mode signals (see "Mixer Implementation" below).

Local oscillator rise time. Fig. 5 illustrates the effect that dc offset in switches (diode match in the ring mixer or V_{BE} match in the active mixer) has on apparent LO symmetry. For purposes of illustration it is assumed that the switch changes state at the dc offset level shown by the dashed line. Even though the zero crossings are symmetrical in the LO signal, switch toggling at the dc offset level results in an equivalent LO waveform that is highly asymmetrical. From inspection it is obvious that as the LO rise time approaches zero, the dc offset no longer alters the times at which the switches change state, and symmetry is preserved.

Switch devices are often nonlinear as they change state.[7] If rise times are short, the influence of these nonlinear transitions is reduced, since less time is spent in transition with respect to the period.

For frequencies at which limiter amplifiers can be implemented effectively, rise time reduction should be pursued. At higher frequencies, where the LO port is driven with a sinusoid, increasing LO power has the effect of reducing the time from LO zero crossing to switch state change.

Mixer Implementation

Fig. 6 shows the schematic diagram of the active mixer in the HP 3326A. Balanced drive is used on both ports as the first measure to ensure balance and reduction of common mode problems.

Variable resistor R_B is used to adjust the balance of the linear pair (Q5 and Q6). Because overall circuit balance, as indicated by minimum RF feedthrough in the IF signal, does not necessarily occur at equal dc collector currents in Q5 and Q6, capacitors C1 and C2 are introduced to prevent a corresponding unbalance in the bias currents of the LO switches (Q1-Q4). By not disturbing the switch bias, a reduction in $2f_{RF} - f_{LO}$ spurious products of as much as 20 dB is achieved. Noting the frequency scheme, this spurious product lies in-band for LO frequencies greater than 27 MHz (output frequencies greater than 7 MHz). The final measure against common mode signals is the inclusion of balun T2.

Differential gain is set (approximately) by the ratio of the sum of the output collector resistors ($R_{C1} + R_{C2}$) to the emitter resistance ($2r_e + 2R_E + R_B$). The 500Ω resistors represent a reasonable maximum value for the combination of gain, noise, and filter realizability.

Transistors Q1 and Q2, Q3 and Q4, and Q5 and Q6 are matched RF devices with typical f_T of 1.5 GHz. They are provided with maximum V_{BE} specifications and guaranteed β match of 80%.

Performance

The following performance is achieved in the HP 3326A's active mixer.

Frequency Scheme
- LO input: 20 MHz to 33 MHz
- RF input: 20 MHz fixed-frequency, level-controlled
- IF output: dc to 13 MHz, differential signal

Harmonic Distortion (typical)
- All harmonics below −90 dBc, dc to 1 MHz at mixer collectors
- Harmonics below −76 dBc to 13 MHz
- Ultimate performance limited by differential-to-single-ended converter

Spurious Responses (typical)
- All spurious products (notably $2f_{RF} - f_{LO}$) better than −90 dBc
- Ultimate overall performance limited by output frequency reinsertion into the mixer, primarily output amplifier current pulses on power supplies

Acknowledgments

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