

Keysight Technologies

Precision Waveform Analysis for High-Speed Digital Communications Using the 86100C and 86108A

Application Note

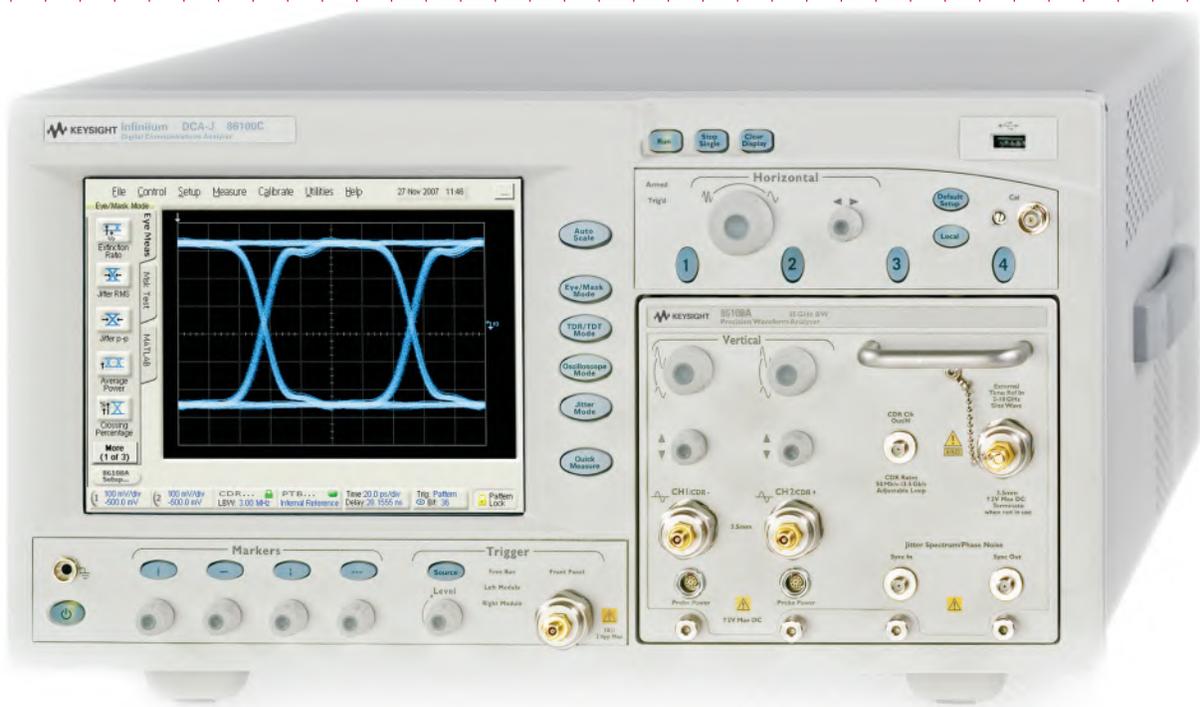


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Introduction

The easiest and most intuitive method for determining the quality of a digital transmitter is to observe the time domain waveform. This is typically done using an oscilloscope. When measuring high-speed digital communications, there are two main choices for oscilloscopes: A real-time oscilloscope and an equivalent time ‘sampling’ oscilloscope. There are distinct advantages for each oscilloscope architecture when compared to the other.

Real-time oscilloscopes:

- Simple to trigger and operate
- Large record lengths/deep memory
- Advanced triggering for observation of infrequent events
- Optimized for troubleshooting scenarios

Sampling oscilloscopes:

- Extremely wide bandwidth
- Low noise and jitter
- Higher resolution analog-to-digital conversion
- Lower cost

No oscilloscope can provide an exact replica of a waveform. This would require the instrument to have infinite bandwidth, zero residual jitter, and no internal noise. However, there are scenarios where it is important to achieve the most accurate waveform possible:

- Design validation versus process, voltage, and temperature
- Providing measurement data for device modeling
- Setting product specifications

This document will discuss using the Keysight Technologies, Inc. 86108A precision waveform analyzer plug-in module with the Keysight 86100C DCA-J sampling oscilloscope main-frame for accurate analysis of high-speed digital communications signals. This system has the optimum combination of bandwidth, noise, and residual jitter to provide what is arguably the most accurate waveform analysis tool available today.

- Bandwidth typically above 35 GHz
- Channel noise typically less than 300 μ V RMS
- Residual jitter typically less than 60 femtoseconds RMS

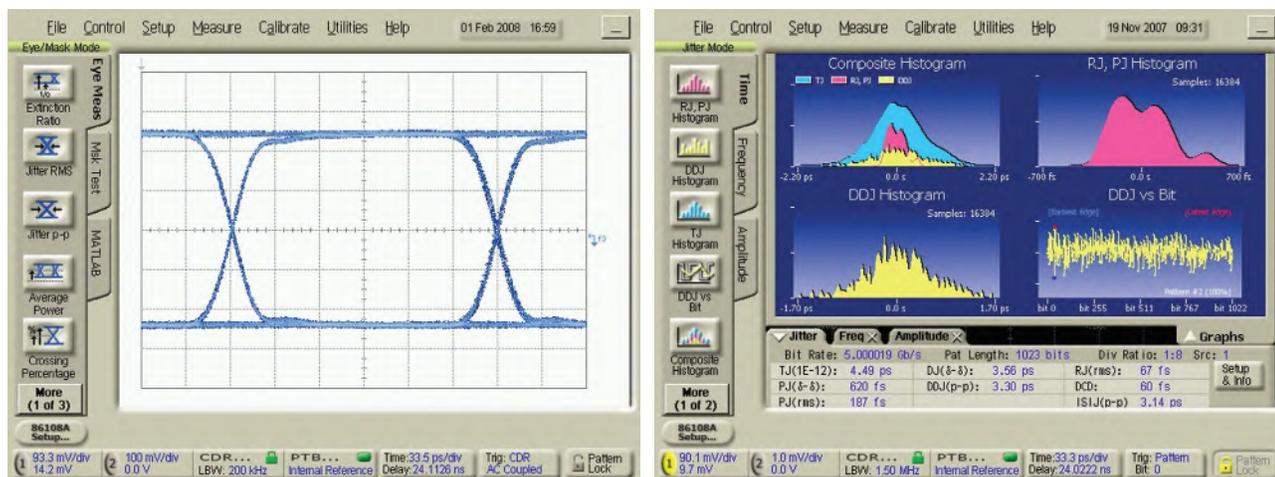


Figure 1: Measurements of a 5 Gb/s signal showing (A) minimal shape distortion, extremely low noise, and (B) a combined (oscilloscope and signal) random jitter (RJ) of 67 fs.

The 86108A Precision Waveform Analyzer

The 86108A is a plug-in module used with the 86100C DCA-J wide bandwidth sampling oscilloscope. The 86108A combines three main functional blocks:

- Two sampling channels
- Integrated hardware clock recovery (data rates 50 Mb/s continuous to 13.5 Gb/s or clock rates 25 MHz continuous to 6.75 GHz)
- Precision timebase

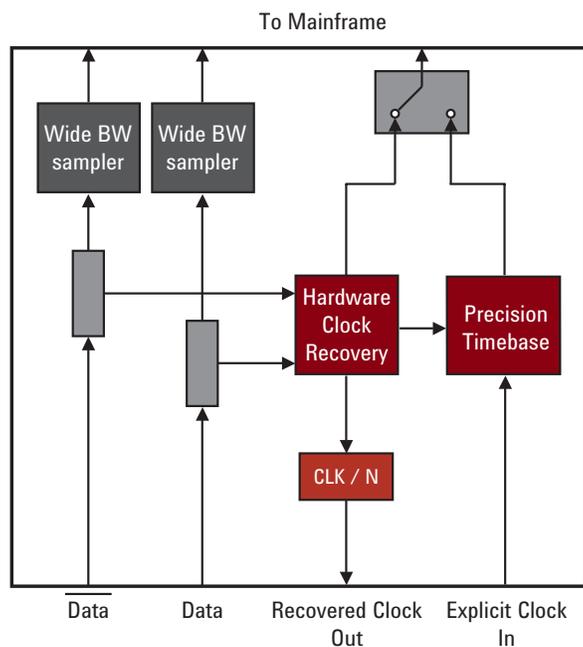


Figure 2: 86108A module and functional diagram

Those familiar with sampling oscilloscopes will recognize that this single plug-in module has the capability that was previously achieved using three separate plug-ins. Obviously this provides both cost and convenience benefits. The requirement of a separate trigger signal to synchronize a sampling oscilloscope can make the instrument more complicated to use than a real-time oscilloscope. An instrumentation grade clock recovery system integrated into the 86108A eliminates this issue. More important than convenience are the improvements in measurement capability achieved through integration. These include:

- A high-integrity ‘single connection’ measurement system. Similar to a real-time oscilloscope, no external signal splitting and extra cabling, which can alter signal performance, are required to make a measurement.
- In addition to ultra-low residual jitter, functional integration virtually eliminates the effects of a large (on the order of 20 ns) trigger-to-sample delay inherent in sampling oscilloscopes. This facilitates accurate measurements of signals employing spread-spectrum clocks and forward-clock systems.

Whether one is familiar with sampling oscilloscopes or not, the 86100C/86108A measurement systems should be considered as the oscilloscope of choice for a “gold standard” of waveform accuracy.

Measurement configurations and procedures using the 86108A

There are several possible configurations for the 86108A

- Single-ended (using one channel) or differential signals (using both channels)
- Triggering through clock extraction from the input signal (single ended or differential)
- Triggering on a user-provided clock

This allows the instrument to be configured for measurements of a variety of serial bus standards including PCI-Express, SATA, FBD, and Quick Path. A user's guide is built into the instrument to quickly take the user through a few configuration steps to insure proper configurations and the best measurements possible. Once familiar with the setups, the guided setup can be skipped.

To launch the 86108A setup, touch/click the 86108A setup key found in the lower left portion of the 86100C screen. The following menu will appear:

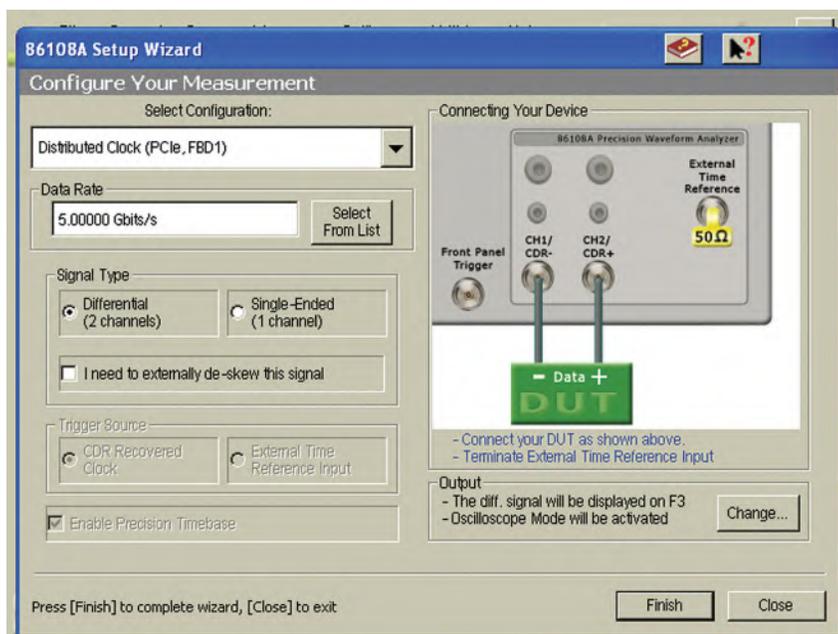


Figure 3: Setup menu for the 86108A

The first step in the guided setup is to select a measurement configuration. Allowable configurations are based on several classes of devices. The instrument settings that are controllable include:

- Data rate
- Single-ended or differential signal input
- Oscilloscope trigger derived from the data using clock recovery or using a user-supplied clock signal
- Precision timebase enabled or disabled

Several measurement configurations are effectively pre-configured and available through the following choices. All choices except 'Custom' have the precision timebase (discussed below) enabled to achieve the lowest residual jitter:

- Embedded clocks (SATA, Infiniband etc). In this configuration the signal being observed has timing information (a 'clock') embedded within the data stream. Waveform measurements will be timed or 'triggered' using a clock extracted from the data stream.
- Forward clocks (FBD2, Hypertransport etc.). In this configuration, system timing information is an explicit clock sent to the receiver. Waveform measurements will be timed or 'triggered' with this explicit clock. This clock is applied to the external time reference input of the 86108A.
- Distributed clocks (PCI-Express, FBD1 etc.). In this configuration, system timing information is derived from a reference clock which is available to the transmitter and the receiver. Waveform measurements will be timed or 'triggered' using a clock extracted from the data stream.
- Ultra-low jitter components: This choice configures the oscilloscope to extract a trigger from the incoming data.
- Custom: This configuration allows the user complete flexibility to configure the instrument including enabling or disabling the precision timebase.

Once the configuration has been determined, the data rate should be entered. The rate can be entered directly by touching/clicking on the data rate value, or selecting a rate from the pre-loaded standard values. (Note that the pre-loaded list can be modified by the user to include new or custom rates).

Note: If clock signals are being observed, the hardware clock recovery system will perceive the signal as a 2-bit pattern at twice the rate of the clock frequency (two bits per clock cycle). Thus if a 2.5 GHz clock is to be measured, the correct entry would be 5 Gb/s.

The 86108A is able to observe either signal-ended or differential signals. The setup allows the choice for the appropriate signal type. When differential is selected, the instrument will configure the internal clock recovery hardware to derive a clock from the differential signal. Also, the system will automatically process the two channel inputs to display the mathematical difference between the signal on channel 2 and the signal on channel 1. For single-ended signals, connect to channel 1.

Accurate displays of differential signals require that timing skew between the two channels be at a minimum. This is particularly true when observing eye diagrams. Skew adjustment must take place external to the oscilloscope using either matched cables or some form of hardware phase trimming device (such as 86108A option 001).

In the 86108A setup page, if the "I need to externally de-skew the signal" is selected, a menu and measurement procedure will be presented to facilitate the de-skew process. This is launched after the "Next" key is selected (discussed below).

Trigger source selections depend on the configuration chosen. With the exception of the “Custom” configuration, the appropriate trigger selection is fixed (but can be changed outside of the setup process). Direct control of either the clock recovery system or precision timebase external clock source is available by touching/clicking the CDR or PTB keys at the bottom center of the oscilloscope display.

A graphic showing the appropriate connections for the selected configuration is shown in the upper right of the 86108A setup menu. Below this graphic is a description of how the resulting waveform will be displayed. This can be altered by pressing the “Change” key. The following menu is seen and allows customization of display and analysis modes:

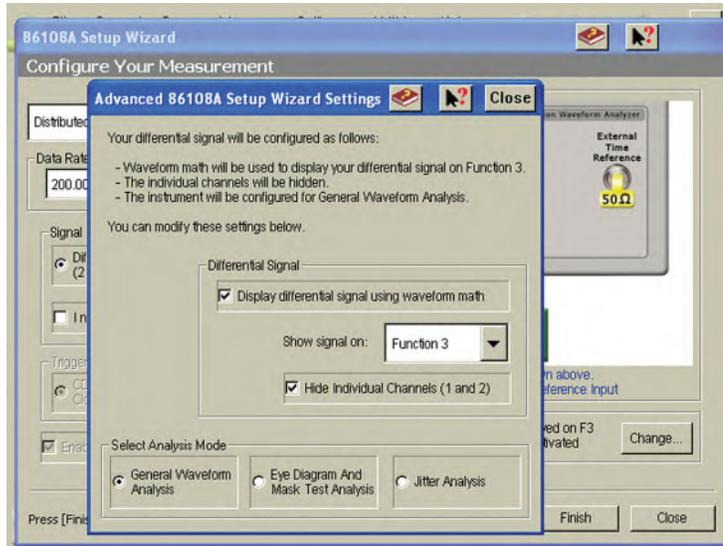


Figure 4: Default configuration of the 86108A system

Once the system has been configured, the “Next” key should be selected. Once this is done, the following steps are automatically performed:

- Pattern length is detected
- A de-skew procedure is launched (if selected in the main setup menu)
- An autoscale is executed

If de-skew was selected in the main setup, the following menu is shown:

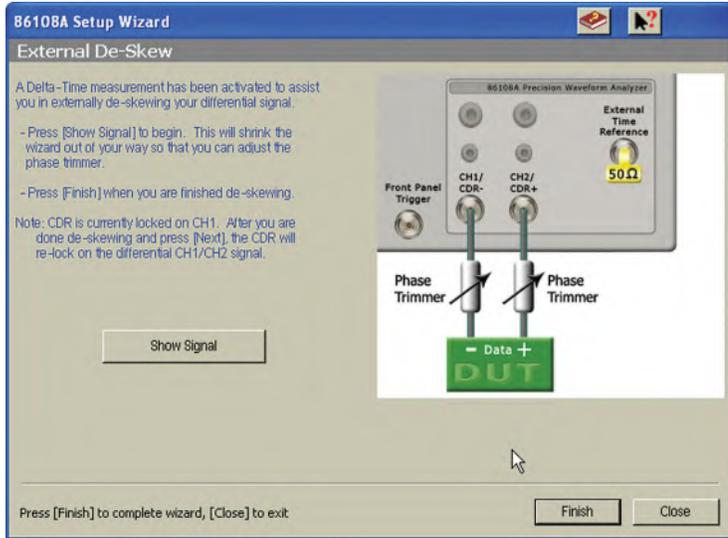


Figure 5: Users guide for channel de-skew

When the “Show Signal” key is selected, the two signals from channel 1 and channel 2 are displayed. A delta time measurement is active which should show the time difference between the first edge of channel 2 and the complementary edge of channel 1. The delta time reading should be minimized through physically adjusting the path length of one leg of the differential signal relative to the other. It is impossible to achieve a 0 delta time value. The target delta time should be near 1 to 2 % of a unit interval or bit period. When the desired skew is achieved press ‘Finish’ to complete the setup.

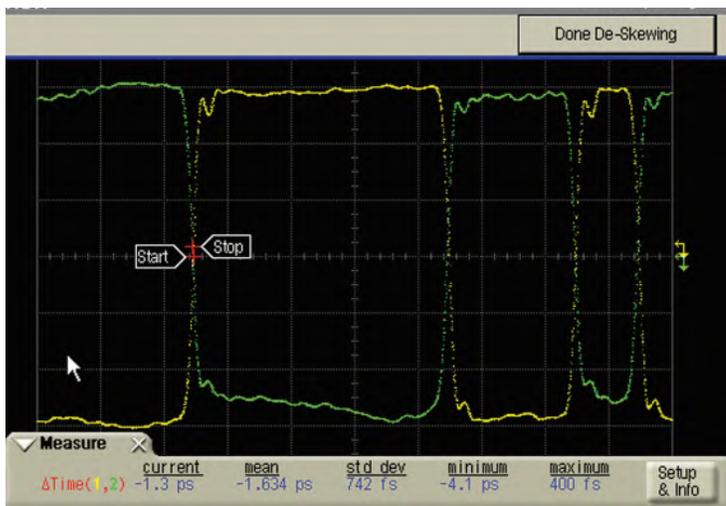


Figure 6: The de-skew process will automatically measure and display the channel to channel skew.

At this point a valid eye diagram or pattern waveform should be on the display. If Jitter Analysis has been selected, a jitter separation will take place and the jitter results, both numerical and graphical will be displayed.

It is also possible to reduce the residual noise of the 86108A system. In the channel controls (press channel 1 or channel 2 in the lower left section of the display) there is an “advanced” section which provides several controls. Sampler bandwidth can be selected at either 20 or 33 GHz. Lowest noise is achieved with the 20 GHz setting. Which setting is best will depend on the signal being observed and which signal parameters are most important.

The 86108A allows several options for triggering the oscilloscope:

- A clock trigger derived from the signal being measured
- User-provided clock trigger to the precision timebase input of the 86108A module
- A trigger (clock, pattern or frame, or edge trigger) provided to the trigger input of the 86100C mainframe

Triggering the oscilloscope (including hardware clock recovery)

Measurement results will be influenced by the triggering signal, as well as where the trigger is applied. Keysight Product Note 86100-5 “Triggering Wide-bandwidth Sampling Oscilloscopes for Accurate Displays of High-Speed Digital Communications Waveforms” (5989-2603EN) provides an in-depth discussion of how the triggering process works in a sampling oscilloscope. This document will review some important aspects of the 86100C/86108A system.

Many 86108A measurements will take advantage of the internal clock recovery system. A clock signal will be derived from the incoming signal and used as the timing reference. Pages 9-13 of Product Note 86100-5 provide a detailed discussion on using a derived clock as a trigger. The clock recovery system in the 86108A is very similar to the 83496B system. The results are summarized as follows:

- Lower frequency jitter from the incoming signal will be transferred to the recovered clock, while higher frequency jitter is not. The clock recovery loop bandwidth setting controls the range of frequencies that transfer.
- Jitter that is common to both the waveform observed and the derived clock is generally not displayed. Triggering with a recovered clock effectively acts as a jitter high-pass function.

The loop bandwidth of the 86108A is adjustable. The range of adjustment is data rate dependent, but has a range from approximately 30 kHz to 10 MHz. Control of the clock recovery system is achieved by pressing the CDR key at the bottom of the 86100C display. There are three areas of control: Input, Clock Recovery, and Output. The Input section allows control of the data rate and whether the input is single-ended or differential. When the system is locked to the input signal, an internal frequency counter accurate to 20 PPM, will display the actual rate of the signal. The Output section allows control of the divide ratio for the recovered clock that is routed to the front panel of the 86108A. The recovered clock that is routed internally for triggering purposes is also divided. Divided triggers can lead to incomplete eye diagrams (see Product Note 86100-5 page 7). However, the 86108A will systematically ‘slip’ the location of the trigger edge relative to the data pattern to allow construction of a complete eye, even when the pattern length is an integer multiple of the divide ratio. In some cases, it is beneficial to trigger on the edges of the data directly rather than from a derived clock. This is achieved by selecting “Trigger on Data”.

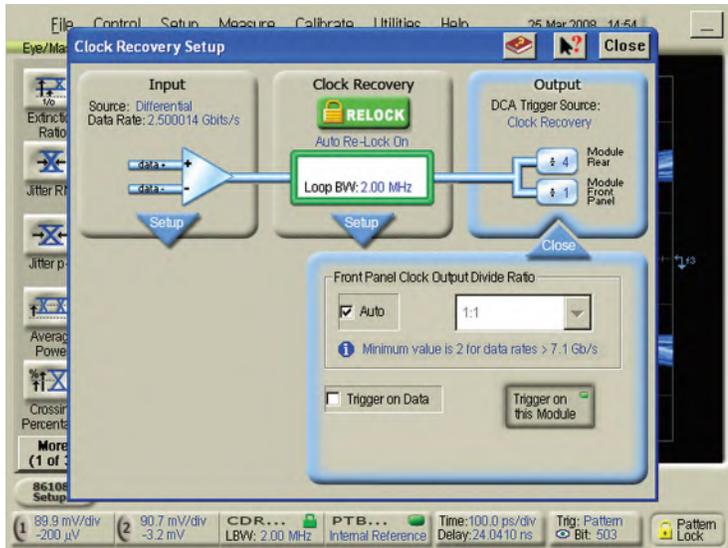


Figure 7: Control menu for the output of the 86108A clock recovery system

Control of the loop bandwidth, and effectively control of the frequency range of observed jitter is in the Clock Recovery section. Two approaches are allowed. In “Rate Dependent” mode, the loop bandwidth is a fixed ratio of the data rate as specified by some communications standards. Default ratios are rate/1667 and rate/2500. For example, if the data rate is 5 Gb/s, and rate/1667 is selected, the loop bandwidth will be 3 MHz. The second mode of operation is “Fixed Value”. In this case, the loop bandwidth is entered directly.

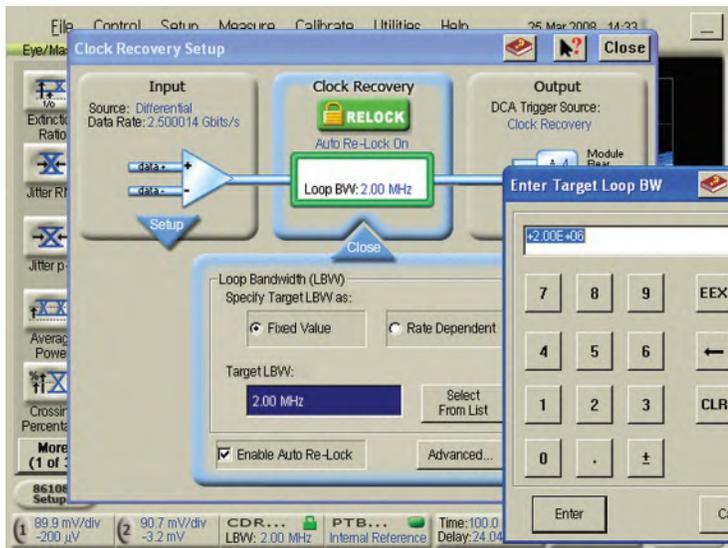


Figure 8: Loop bandwidth control of the 86108A clock recovery system

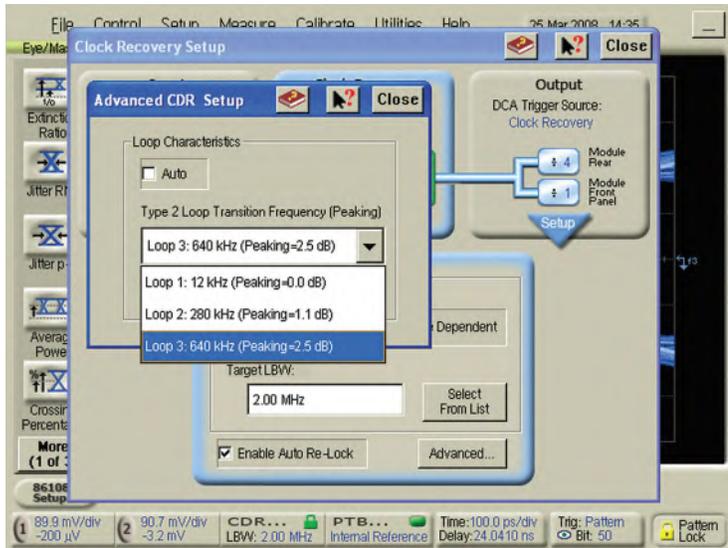


Figure 9: Peaking control for the 86108A clock recovery system

Some communications standards require a specific 'peaking' characteristic in the loop design. Control of the peaking is available in the Advanced section of the Clock Recovery control.

When hardware clock recovery is used, the system will lose lock whenever a signal at the expected rate is no longer present at the oscilloscope input. When the signal returns, a lock can be achieved by manually pressing RELOCK. However, for convenience, an Auto Re-Lock can be enabled that will re-lock the system and resume acquisition when the signal becomes available. This is a useful feature for scenarios where signals are frequently interrupted (such as circuit probing).

Low jitter measurements using the precision timebase (PTB)

The ultra-low residual jitter of the 86108A is achieved through the PTB. Without the PTB, the residual jitter of the oscilloscope is approximately 750 fs. With the PTB the residual jitter is typically less than 60 fs. Very few signals have jitter this low. Thus for most measurements, the oscilloscope is effectively jitter free. For example, if a signal has a random jitter of 200 fs RMS, the oscilloscope would measure ~208 fs. The error due to residual oscilloscope jitter is only 8 fs.

Figure 10 shows an eye diagram measured with the 86100C/86108A system. The signal is measured with the PTB disabled.

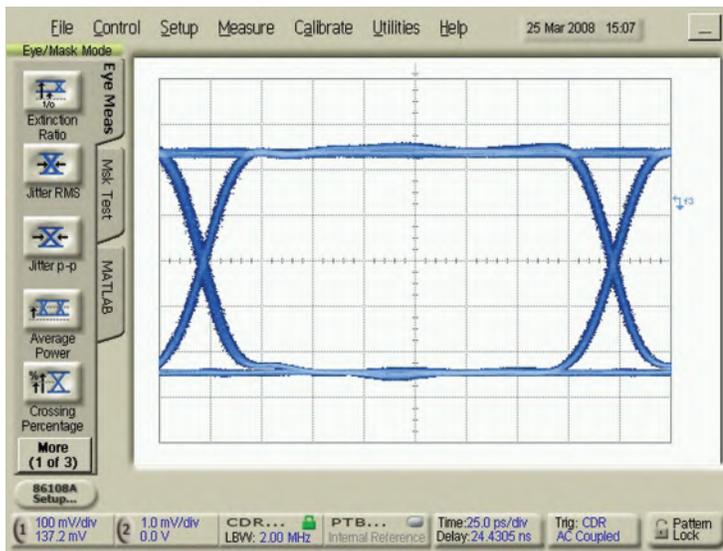


Figure 10: Eye diagram analysis in a 'common' sampling oscilloscope configuration

The signal is measured again with the PTB enabled. Both eye diagrams show a very good signal, but it is clear that the jitter observed visually as the width of the eye crossing, is less in the PTB enabled waveform (Figure 11).

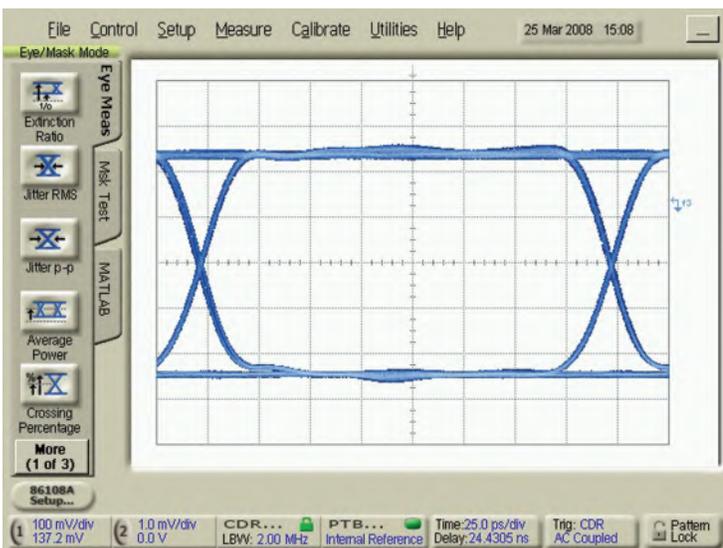


Figure 11: Eye diagram analysis with the 86108A precision timebase enabled

The apparent differences between a PTB enabled or disabled waveform are subtle. Expanding the waveform to a higher resolution reveals better insight. When the PTB is disabled, the widths of the populations of rising and falling edges of the eye appear random. The various trajectories have what appears to be a Gaussian distribution, typical of a signal dominated by random jitter.

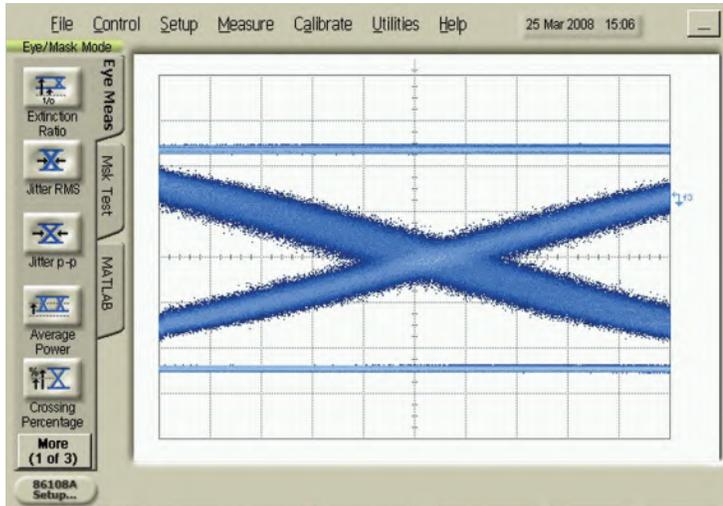


Figure 12: Eye diagram crossing point with 86108A precision timebase disabled

However, when the PTB is activated, the signals trajectories appear quite different. There are two distinct groupings of falling edges previously not observed. (In fact a very close inspection reveals several distinct trajectories in both the rising and falling edges). Rather than random jitter, deterministic jitter is the true dominant jitter mechanism for this signal. This phenomenon cannot be observed unless the random jitter of the oscilloscope is reduced to a very low level. Otherwise, the residual jitter of the oscilloscope obscures the true signal performance.

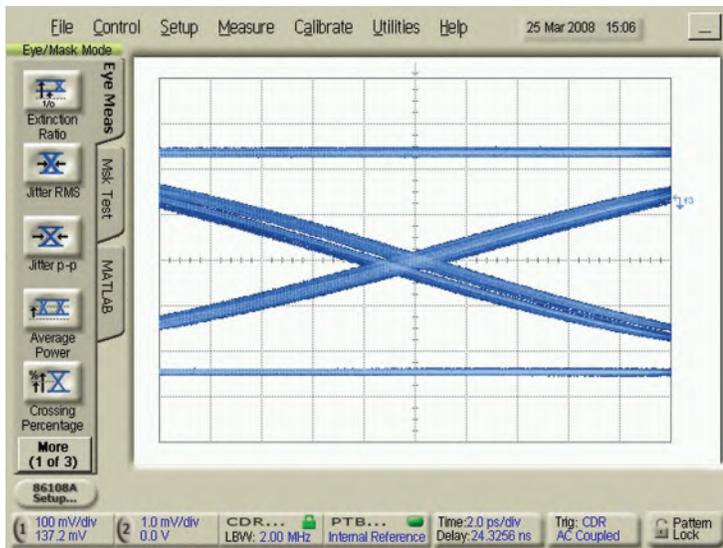


Figure 13: Eye diagram crossing point with precision timebase enabled

The PTB is a system that effectively measures the phase of a clock trigger (provided from the clock recovery system or using a clock signal at the PTB front panel). This allows an extremely accurate determination of the relative time at which a sample is taken, since the PTB system is precisely synchronized to the firing of the samplers of the measurement channels.

When using a clock at the PTB front panel, best precision is achieved when the signal is sinusoidal. Although the PTB system is very tolerant of non-sinusoid clocks, square wave clocks should be avoided, or should be low-pass filtered to suppress harmonics of the fundamental frequency. When using the clock recovery system, a sinusoidal clock is provided internally to the PTB.

The PTB can be enabled or disabled through the PTB menu key located at the bottom of the 86100C display.

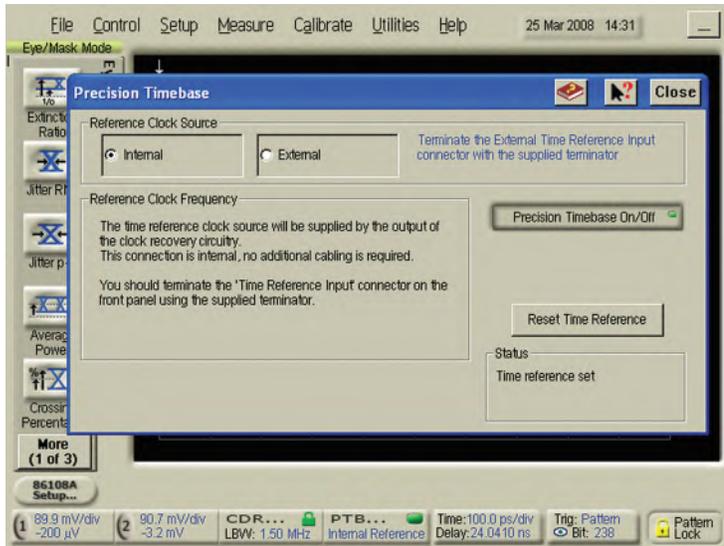


Figure 14: Precision timebase control menu

The PTB system can drift if the oscilloscope has just been turned on and its temperature is changing. This can be observed as a waveform that is shifted on the display and has no sample points on the left side of the graticule. If this occurs, the “Reset Time Reference” key will re-synchronize the system. Once temperature stable, drift should be minimal.

Note: When using the clock recovery system as the timing reference, the PTB front panel input should be terminated in 50 Ohms.

Achieving zero trigger delay

An important benefit provided by the PTB, beyond the reduction of residual oscilloscope jitter, is mitigation of the delay between the trigger event and when a waveform sample is taken. In the common sampling oscilloscope configuration, when a trigger event occurs, at least 20 ns elapse before a waveform sample is acquired. (The time between the trigger event and the sample time is shown as the 'Delay' value in the timebase settings of the oscilloscope (lower right section of the 86100C display)).

When the PTB is used, there are effectively two levels of synchronization used in the oscilloscope system. There is the classic 'trigger event' that initiates the sampling process. There is also the concept of a synchronization signal that determines where samples are positioned on the instrument display relative to each other. In the common sampling oscilloscope, the trigger event and the synchronization signal are identical. The trigger event initiates the sampling process. Sample points are displayed relative to the same trigger event. However, when the PTB is enabled, data samples as well as the synchronizing clock provided to the PTB (from the clock recovery system or as a direct input to the PTB input port) are measured simultaneously. This allows the sampled data to be displayed with virtually no delay between the oscilloscope synchronization signal and data samples. Samples are displayed synchronized and completely correlated to the triggering clock. The timebase delay value will still indicate a value in excess of 24 ns. This term indicates the time between when the sampling process is 'triggered' and when the sampling actually takes place. However, from the perspective of the displayed waveform, there is no delay between the clock and the sample.

A large trigger to sample delay is often not a problem, but can become a significant problem when there is jitter on both the signal being observed and the clock used to trigger the oscilloscope. This is discussed in detail in Product Note 86100-5 pages 14-15. When jitter is common to both the trigger and the data, they tend to track each other and the observed jitter is suppressed. However, if there is delay between when the oscilloscope is triggered and when the sample occurs, the tracking effect is altered. In the most extreme case, observed jitter can be double the actual value. A 'zero delay' measurement eliminates this issue. Jitter is observed correctly.

It is important to note that a 'zero delay' sampling oscilloscope can be achieved using separate clock recovery, PTB, and measurement channels. However, in practical terms this is very difficult to achieve. Signal path lengths to the various system elements have to be precisely matched. Even seemingly small mismatches result in large measurement errors, especially when signals with large jitter components are observed. This is most critical when observing signals that employ spread-spectrum clocks.

Measurements of signals employing spread-spectrum clocks (SSC)

The trigger-to-sample delay is critical when signals using SSC are observed. SSC systems intentionally apply a low frequency (e.g. 33 kHz) frequency modulation on the signal to distribute radiated energy across a broad spectrum. This is essentially intentional jitter. This low frequency jitter is often performed at very large amplitudes. That is, a given edge position can deviate many unit intervals from its ideal (jitter free) position. If the signal eye diagram is observed using an oscilloscope triggered with a clean (jitter free) clock, the jitter is so large that the eye diagram will be completely closed.

It is difficult to get much useful information from a closed eye. Clock recovery can be employed to allow the oscilloscope to 'track out' the SSC effects and observe the other important characteristics of the signal. Some standards specifically dictate that the clock recovery system have the ability to suppress the SSC by 72 to 75 dB. Essentially the observed jitter transfer (discussed in Product Note 86100-5 pg 10 and 14) has extremely low transfer at SSC frequencies. Trigger-to-sample delay will reduce the suppression of SSC. Suppression will still be significant, and some eye opening is likely to be achieved, but significant SSC will still be present.

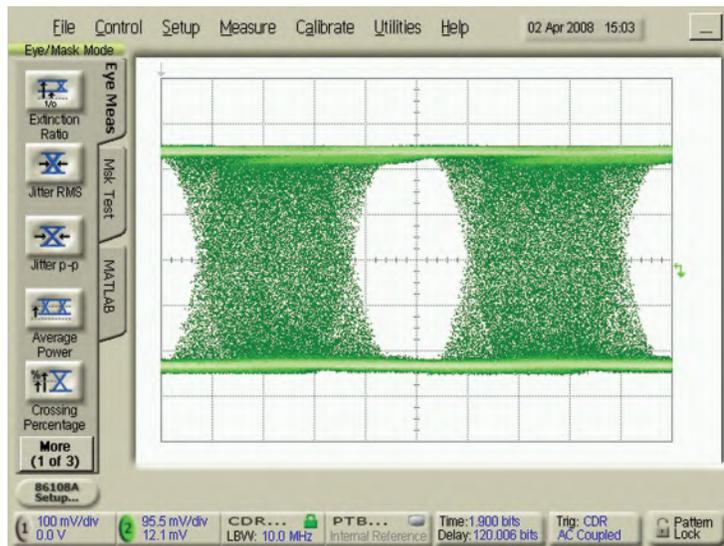


Figure 15: Display of SSC signals using an extracted clock trigger with typical sampling oscilloscope delay (~24 ns, or 120 bits at 200 ps/bit)

With the 86108A system, the trigger-to-sample delay is effectively zero when the precision timebase is enabled. The desired SSC suppression of approximately 74 dB is achieved and virtually the entire SSC component is tracked out from the observed waveform.

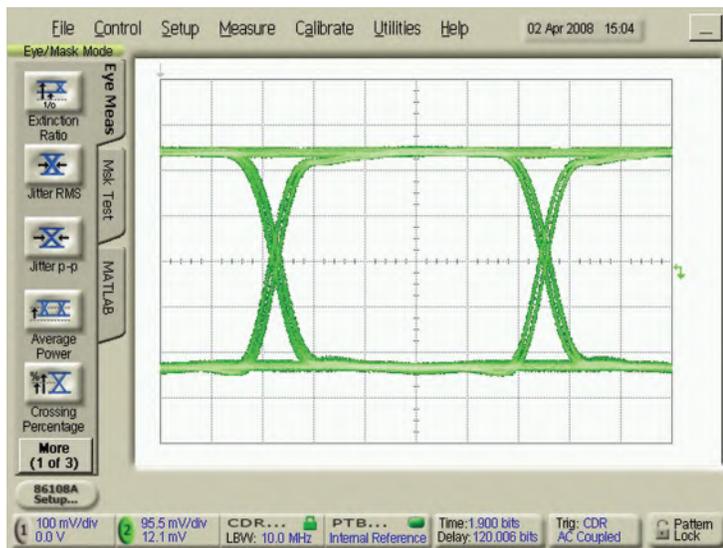


Figure 16: SSC suppression achieved with high-gain clock recovery and 0 trigger-to sample delay

An interesting effect is observed when an SSC waveform is measured using high-gain clock recovery, the oscilloscope has very low residual jitter, and there is no trigger to sample delay. When all these conditions are met, the SSC, after ~74 dB of suppression, is seen as bimodal jitter on the eye diagram or on any data edge.

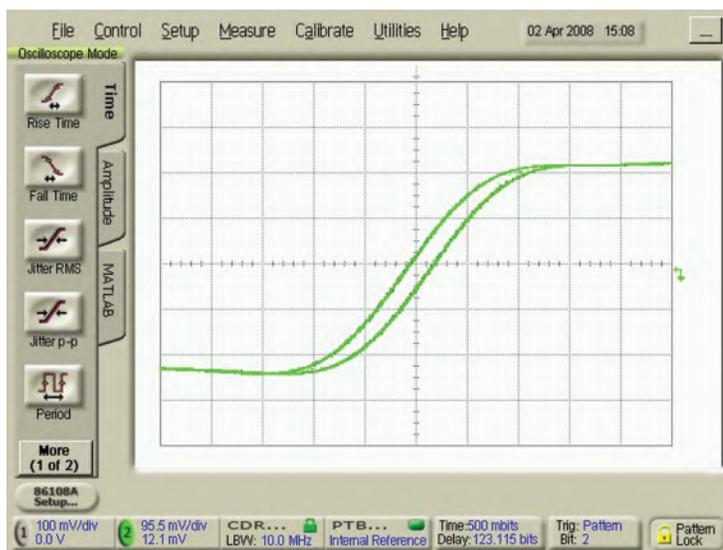


Figure 17: Observing SSC on a rising edge. SSC exhibits a bimodal edge when observed under ideal conditions.

SSC is usually implemented using a triangle wave frequency modulation. The distribution of triangle wave jitter should be uniform, not bimodal. The standards specified second order type 2 phase locked loop results in a 40 dB per decade observed jitter transfer function which is required to achieve high SSC suppression. The second order loop results in a phase error signal that is the derivative of the triangular FM waveform. The resulting eye diagram will have a bimodal jitter distribution due to the SSC. Trigger-to-sample delay and/or other jitter components (such as random jitter) have a tendency to smear the jitter distribution and may mask the expected bimodal display. Since the 86108A has zero trigger delay and low residual jitter, the bimodal effect is easily observed, especially on the edge of a data pattern waveform.

Note that SSC tracking does not remove all the jitter. In the following example, a high quality signal with SSC is observed. The expected bimodal edge is seen (this time in the eye diagram crossing point). However, the jitter distribution is not as distinct as with the edge shown in figure 18. This is due to a small amount of pattern dependent jitter present on the signal, which partially obscures the bimodal display of residual SSC. If there is significant jitter present that is at rates beyond the loop bandwidth of the clock recovery system, the residual SSC may be difficult to observe, except in 86100C Jitter Mode, where its effect can be separated from other jitter components and displayed both graphically and numerically as a periodic jitter contribution.

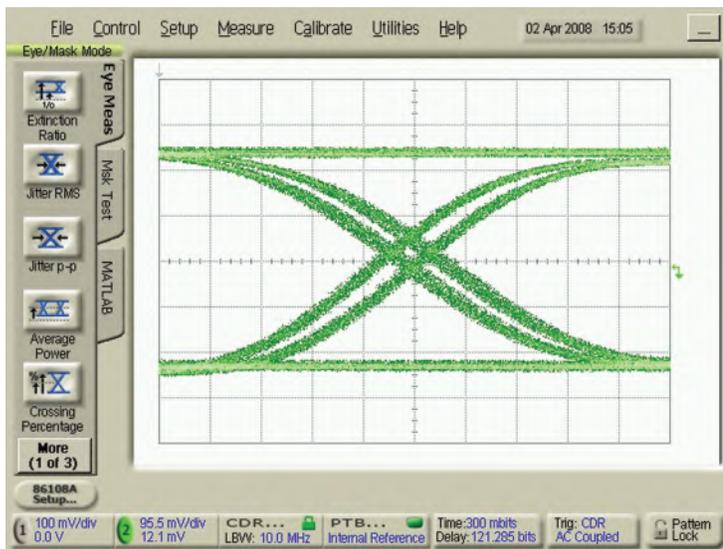


Figure 18: Eye diagram crossing point observed when both SSC and data dependent jitter is present.

A deep memory sampling oscilloscope

While sampling oscilloscopes provide better bandwidth, noise, and residual jitter than real-time oscilloscopes, the number of sample points that can be achieved in a single acquisition are comparatively very low. The typical maximum record length (number of sample points in a single waveform acquisition) is under 5000 points. Firmware revision 8.0 will allow the 86100C to have a maximum record length of 16384. This is still very small compared to the best real-time oscilloscope, currently at 1 billion points. Oscilloscopes capable of providing long waveform records are referred to as having deep memory.

Deep memory is beneficial to any analysis that requires a waveform record of a long data sequence. Device and system performance can often vary according to the data sequence and may not be observed unless the data sequence is very long. Eye diagrams allow analysis of long patterns even with short record lengths, as many individual waveform acquisitions can be overlaid on a single waveform display. However, some analysis techniques cannot be achieved using an eye diagram. A long continuous waveform record is required.

The individual bits of a waveform can be displayed with any sampling oscilloscope if it is triggered with a 'pattern trigger' (see PN 86100-5 page 5). However, even with a record length of 16384 it is difficult to observe a long waveform record with much precision. The 86100C can be configured to provide the accuracy benefits of a sampling oscilloscope with an effective deep memory. The 86100C (with option 001) has the ability to automatically synchronize to any repeating data pattern up to 223 bits in length. (It has the ability to create the equivalent of an internal trigger that locks to the repetition rate of the data sequence). This allows the oscilloscope to display the individual bits of a pattern rather than a composite eye diagram. To achieve a long waveform record, the 86100C option 201 software will automatically sequence through the pattern, acquiring a precision record of each bit (at up to 4096 points per bit). The segments of the waveform are then aggregated to yield a single continuous record that is stored on the mainframe hard drive.

Intuitively, the process could be viewed as capturing the first bit of a pattern and saving that waveform. The oscilloscope timebase is then delayed precisely one bit period in time to observe the next bit in the pattern. The second waveform is added to the first for a new waveform twice the length as the first. The process is repeated until the entire pattern has been observed and a long waveform record has been created. However, there is an important accuracy problem to consider in this process. With each succeeding bit record, the oscilloscope is performing its acquisition further and further away in time from the triggering event. Any nonlinearity in the oscilloscope timebase will manifest itself as distortion of the waveform.

The 86100C-201 pattern waveform process has a distinct difference from the process described above. Rather than sequencing through the waveform by increasing the timebase delay, the 86100C-001 acquisition system adjusts its sampling time so that the appropriate bit is observed, but with an almost fixed timebase delay value. This delay value is chosen to be at the most linear region of the oscilloscope timebase. The result is a deep memory acquisition with the highest waveform precision.

To save a long waveform record, the 86100C must first be in "pattern lock" mode. Select the pattern lock key at the lower right of the display (the 86108A setup sequence may have already performed this process. If it has, the pattern lock key will be highlighted). In the upper toolbar press File/Save/Pattern Waveform.

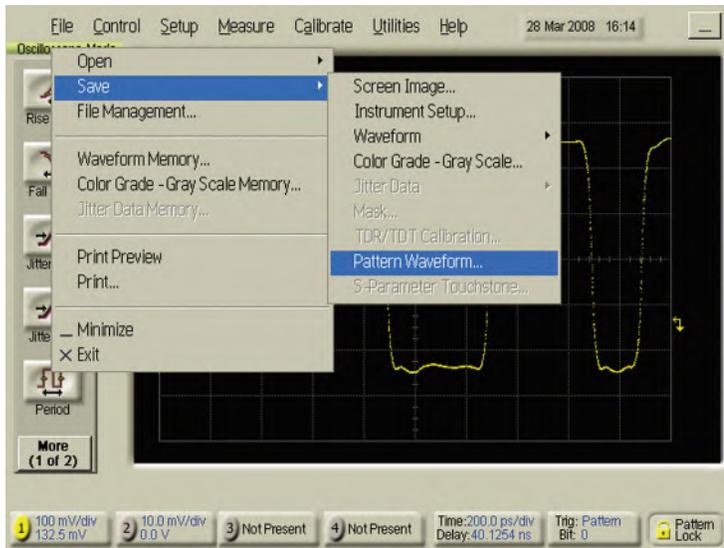


Figure 19: Pattern Waveform file save menu

The following menu will appear:

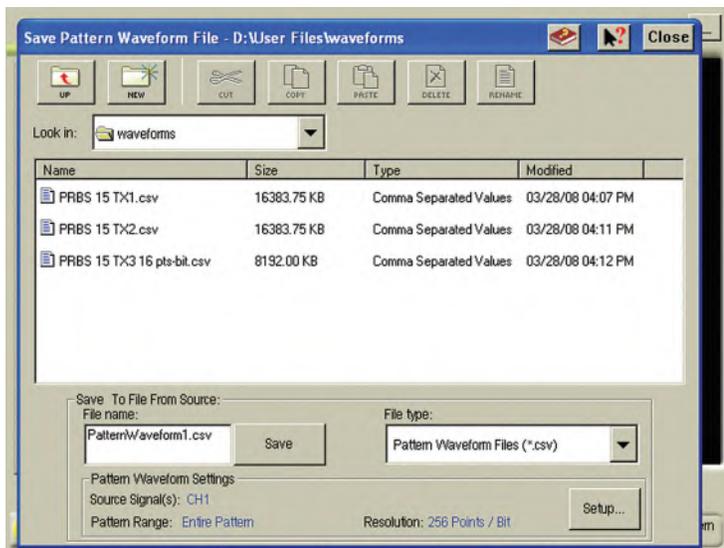


Figure 20: File save menu continued

Pressing the setup key, a new menu will appear:

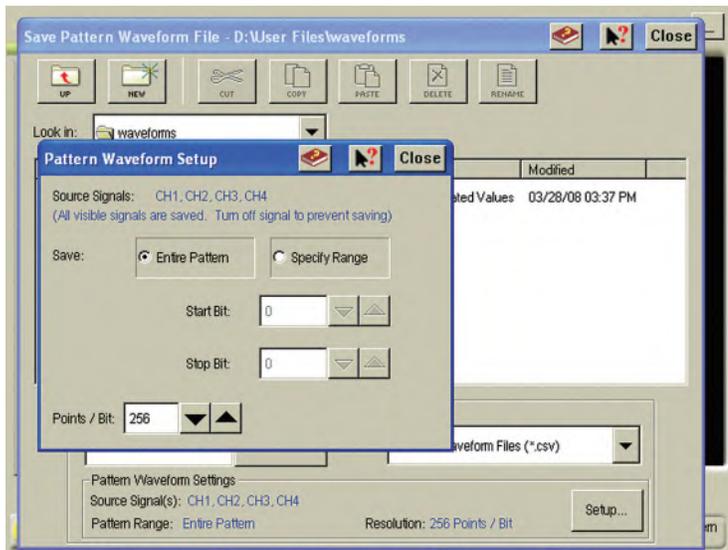


Figure 21: Setting up the points per bit and pattern capture

The waveform save process allows either the entire pattern or a subset to be saved. All active display channels, sampled synchronously, can be saved. (Note that the start location of the pattern is somewhat arbitrary, as the oscilloscope cannot identify a true beginning or ending to the pattern). The number of sample points per bit is also user-definable, with a maximum of 4096 points per bit. Once this is configured and a waveform filename is entered, the system will automatically perform the acquisition.

The file is stored as a 'comma separated variable' or .csv file.

Jitter spectrum and PLL bandwidth/jitter transfer analysis

The clock recovery system of the 86108A includes a high performance phase detector. The output of the phase detector is effectively the demodulated jitter of the incoming data or clock signal. Through monitoring the phase detector output, the phase noise and jitter spectrum can be observed.

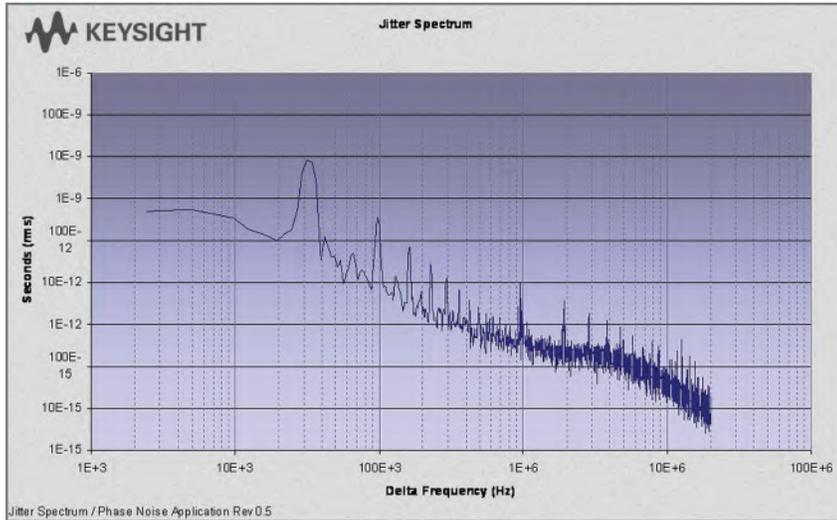


Figure 22: Frequency domain display of baseband jitter

By observing the jitter in the frequency domain, it is often easy to detect the root causes of jitter. (Discrete tones are indicators of sources of periodic jitter. Knowing the frequencies of the periodic jitter leads to its sources.) Random jitter has a broad spectrum with no discrete tones. The spectral floor of the jitter indicates what mechanisms are generating random jitter.

When combined with a jitter stimulus (such as the N4903 JBERT), the 86100C/86108A system can determine PLL bandwidth and jitter transfer performance. The system allows clock or data inputs and clock or data outputs and thus can test a variety of devices including clock recovery systems, repeaters, clock multipliers, and PLL based transmitters.

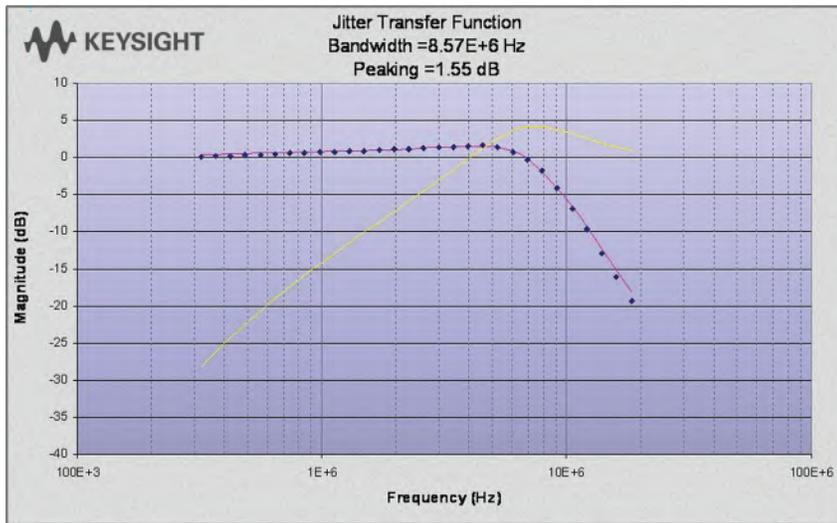


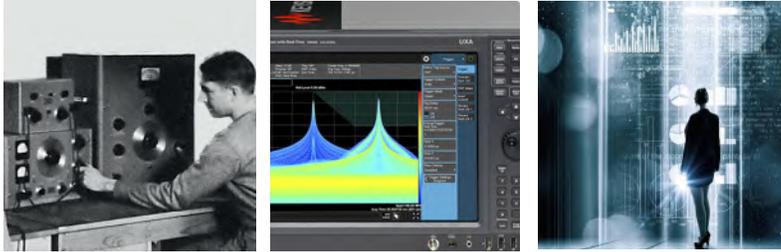
Figure 23: Jitter transfer and observed jitter transfer response

Please refer to Product Note 86100C-2 Solving Jitter Problems Through Jitter Transfer/ Loop Bandwidth, Jitter Spectrum and Phase Noise Analysis (5989-6551EN available May 2008) for details.

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