TELECOMMUNICATIONS TEST EQUIPMENT

Dedicated 150 Mb/s PCM/TDM Error Detection System

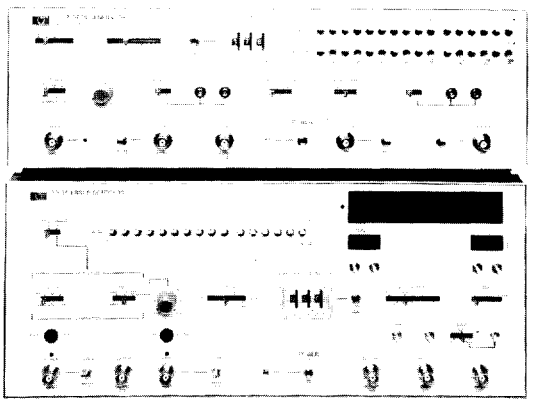
Models 3762A/3763A, 3764A

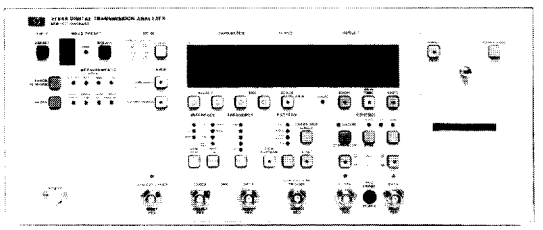
HP 3762A/3763A
- Binary bit-by-bit error detection
- Coded and binary operation
- Variable clock frequency offsets

HP 3764A
- Full 140 Mb/s error measurement
- Jitter generation and measurement at 140 Mb/s
- Portable single-unit construction

HP 3762A

HP 3763A





HP 3764A

DESIGNED FOR HP-IB SYSTEMS

HP 3762A Data Generator/3763A Error Detector

The HP 3762A Data Generator and HP 3763A Error Detector comprise a dedicated error rate measurement system for evaluating high-speed digital transmission equipment. Basically, there are two versions of the system available. One features CMI and binary data formats and is specifically intended for use in field commissioning and maintenance of digital radio (terrestrial microwave and TDMA satellite) systems. The other version, with CMI and ternary (HDB3 and B3ZS) data formats, is designed for digital multiplex and digital cable systems. Burst gating inputs allow the HP 3762A/3763A to be used in TDMA applications

Specifications Summary

HP 3762A Data Generator

Internal clock: two crystal clocks in the range 30 to 150 MHz; crystals fitted in standard unit are 139.264 and 141.040 MHz; offset continuously variable up to ± 60 ppm.
External clock input: 1 kHz to 150 MHz; 75 ohm.
Patterns: $2^{10}-1$, $2^{15}-1$, and $2^{23}-1$ PRBS; two 10- or 16-bit programmable words: two 1010 . . . repetitive patterns; two 8-bit words alternated by an external signal; PRBS patterns can be gated off for 1 to 999 clock periods after trigger pulse (zero substitution); error add facilities.

HP 3763A Error Detector

Data input: CMI, NRZ, or RZ formats; 75 ohm; DATA or $\overline{\text{DATA}}$; 12 dB fixed equalization at 70 MHz on CMI inputs with clock recovery.
External clock: as 3762A.
Patterns: all the patterns of the HP 3762A, including zero substitution, but excluding alternating words.
Count: totalizes errors over a selected gating period; internal period can be 10^6, 10^8, 10^{10} clock periods or 1 min to 24 h, repetitive or single shot, manual start/stop or external (ECL) control; result displayed as ABCD.
Measurement gating input: gates error and clock inputs to error counter, providing a measurement "window"; 50 ohm; ECL levels.
Frequency offset measurement: measures deviation of received bit rate from nominal rate; result displayed as ± BCD × 10^{-6}.
Printer output (rear panel): 8-4-2-1 BCD, 10-column output of result plus local time, if required, and flags; TTL print command pulse.
Recorder output (rear panel): constant current drive output of BER or COUNT result, with flags.

Ordering Information	Price
HP 3762A Data Generator	$8,660
HP 3763A Error Detector	$7,850

HP 3764A Digital Transmission Analyzer

The HP 3764A Digital Transmission Analyzer is Hewlett-Packard's new product for analyzing the error performance of high speed digital transmission systems. Three versions of the HP 3764A are produced, each being designed to fulfill different operating requirements. This flexible approach allows the HP 3764A to provide substantial benefits in a wide range of applications, from design and development to commissioning and maintenance.
- Standard HP 3764A — this is a dedicated 140 Mb/s digital transmission analyzer with pattern generation, error detection and error analysis capabilities. The error analysis provision includes error performance measurements for testing the proposed Integrated Services Digital Networks (ISDN).
- Multiple frequency version — option 001 instruments provide the standard HP 3764A's measurement capability at the four main CEPT bit-rates of 2, 8, 34 and 140 Mb/s. This reduces the number of test sets required in multiple frequency environments.
- Jitter version — in addition to the standard HP 3764A's measurement capability option 002 instruments also provide jitter generation and timing jitter measurement at 140 Mb/s. This offers a cost-effective solution to 140 Mb/s testing requirements.

Specifications Summary

Generator Section

Clocks: internal clock 139.264 MHz; offset clocks + and − 15 ppm; external clock 1 kHz to 170 MHz.
Data outputs: CMI format at 139.264 Mb/s; Binary RZ or NRZ from 1 kb/s to 170 Mb/s, ECL levels, 75 ohm unbalanced.
Patterns: PRBS $2^{23}-1$; WORD, 1 to 16-bit fully programmable; ALT WORD, two 1 to 8-bit programmable words, crossover rate controlled by external signal; AIS, "all ones" pattern.

Receiver Section

Recovered clock: 139.264 ±3 Mb/s.
Binary clock: 1 kHz to 170 MHz.
Data inputs: 75 ohm Terminated mode: Monitor mode; Binary, RZ or NRZ, ECL levels; External Error, ECL levels.

Measurements Performed

Error performance: % Availability, % ER <= N, % EFS.
Errors: Error Ratio, Error Count, Error Seconds, Error Free Seconds.

Options	Price
(Select one option only)	
001: four internal frequencies.	+$750
002: jitter generation and measurement at 140 Mb/s.	+$2,570
HP 3764A Digital Transmission Analyzer	**$9,630**