INTRODUCTION

The PJM-4 is a compact jitter meter which makes use of the most modern technology. It can be used to measure jitter on clock and data signals in the frequency range 700 kbit/s to 16800 kbit/s. Sinusoidal-, rectangular-, triangular- and sawtooth (duty cycle 50%) clock signals can all be measured, as can data signals with the following line codes: HDB3, B6ZS, B8ZS, CMI, 1B2B, 4B3T, 5B6B, AMI, NRZ (TTL/ECL) and RZ (TTL/ECL).

The built-in code error counter can be used for monitoring the transmission path for code errors. All of the above-mentioned codes can be monitored in this way.

The phase hit counter is used for registering all phase hits which are above a threshold value which can be set to your own requirements.

Some important features of the PJM-4

- It fulfils or is better than the requirements for jitter meters laid down in CCITT Recommendation O.171
- Five fixed bit rates are provided as standard. A further 4 bit rates can be provided to your own specifications
- External clock range extends from 0.7 to 168 MHz without any gaps
- Code error analysis for all the line codes mentioned above. The line codes 4B3T and 5B6B, however, can only be evaluated if this option is fitted (charged extra)
- Phase hits are registered over a given threshold and gate time (both variable), as absolute and relative values.
- The PJM-4 can be fully integrated into ATE systems. It has excellent synchronisation performance and is capable of very rapid jitter measurements
- A wide range of low- and high-pass filters are built in to the instrument. The filters can be combined as required, and you can also connect other filters via the external inputs.
- All instrument functions can be remote-controlled via the IEC 625/IEEE 488 bus system. The PJM-4 can itself control an IEC bus compatible printer.

1.1 BIT RATES

Up to 9 fixed bit rates can be provided by fitting the appropriate crystal oscillators into the instrument.

Built-in standard bit rates:

BN 2019/01 ..... 2048, 8448, 25776, 34368 and 139264 kbit/s
BN 2019/02 ..... same as BN 2019/01
BN 2019/03 ..... 1544, 3152, 6312 and 44736 kbit/s
BN 2019/04 ..... 1544, 3152, 6312, 32064 and 97728 kbit/s

Additional bit rates (option BN 2019/00.10)

Four or five further user-specified bit rates in the range ..... 700 kbit/s to 168 Mbit/s

External clock feed

External synchronisation of the instrument to bit rates other than those internally generated.

Frequency range ..... 0.7 MHz to 168 MHz
Clock input (back panel) ..... BNC socket
Impedance ..... 75 Ω
Peak-to-peak input voltage required ..... 0.5 to 4 V
Maximum peak-to-peak input voltage ..... 10 V

Pulling range limits

Allowable deviation of the bit rate to be measured from the internal clock frequency to the externally supplied clock frequency ..... ± 75 ppm

1.2 BIT PATTERNS

1.2.1 BIT PATTERNS WHICH CAN BE ANALYSED FOR JITTER MEASUREMENTS

Clock jitter measurements
(input switch set to CLOCK)

Squarewave signals with a duty cycle of 50% or sinusoidal signals can be handled.

Repetitive patterns, line code RZ (TTL/ECL) ..... sequence ...1111...
NRZ (TTL/ECL) ..... sequence ...1010...
CMI ..... sequence ...0000... or ...1111...

Data signal jitter measurements
(input switch set to DATA)

For HDB3 (HDB2), CMI, 4B3T and 5B6B line codes ..... any pattern

For AMI, NRZ (TTL/ECL) and RZ (TTL/ECL) line codes ..... repetitive patterns with not more than 15 missing zeros, or pseudo random bit sequences up to 2^{23}-1 bits long.

1.2.2 BIT PATTERNS WHICH CAN BE ANALYSED FOR CODE ERROR COUNTING

Code error recognition for line codes ..... CMI, AMI and HDB3

Additionally, with option BN 2019/00.01 ..... 4B3T, 5B6B

1.3 S I G N A L I N P U T *

Input impedance ..... 75 Ω

Input impedance for NRZ/ECL and RZ/ECL line codes referred to ..... -2 V

Return loss between 25 kHz and 210 MHz ..... ≥ 20 dB

Input voltage

Maximum allowable input signal amplitude ..... 7 V

Peak input voltage for pulse or sine signals

Input equaliser

in "flat" setting ..... ± 50 mV to ± 3 V

in "$\sqrt{f}$" setting ..... automatic equalisation of frequency dependent cable losses in accordance with the $\sqrt{f}$ rule. The nominal amplitude is either entered using the decimal keypad, or is automatically set to a value recommended in CCITT 0.171 for the particular bit rate/line code combination.

Maximum equalisation at 70 MHz ..... 12 dB

Range of entry for pulse amplitude value ..... ± 100 mV to ± 3 V

1.4 J I T T E R M E A S U R E M E N T

Measurement range ..... 0 to 15.99 UI_{pp}

Resolution, 0 to 1.999 UI_{pp} ..... 0.001 UI

2 to 15.99 UI_{pp} ..... 0.01 UI

1.4.1 JITTER FREQUENCY RANGE

1.4.1.1 Weighting filter

Manual or automatic selection to CCITT Rec. 0.171.

Available high pass filters

3 dB cutoff frequencies at ..... 2 Hz, 10 Hz, 20 Hz, 60 Hz, 100 Hz, 200 Hz, 700 Hz, 3 kHz, 8 kHz, 10 kHz, 18 kHz, 24 kHz, 32 kHz, 80 kHz, 160 kHz, 900 kHz

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* Versacon® 9 basic 75 Ω connector fitted with BNC insert

High pass filter attenuation characteristic in stop band

2 Hz high pass filter ..... 40 dB per decade

all other high pass filters ..... 20 dB per decade

Available low pass filters

< 0.1 dB attenuation at	3 dB cutoff at
40 kHz	74 kHz
100 kHz	185 kHz
160 kHz	300 kHz
400 kHz	600 kHz
800 kHz	1.2 MHz
4.5 MHz	6.7 MHz

Low pass filter attenuation characteristic in stop band ..... 60 dB per decade

Weighting using external filters

Output and input (back panel) ..... BNC sockets

Characteristic impedance ..... 75 Ω

Nominal pass band attenuation ..... 6 dB

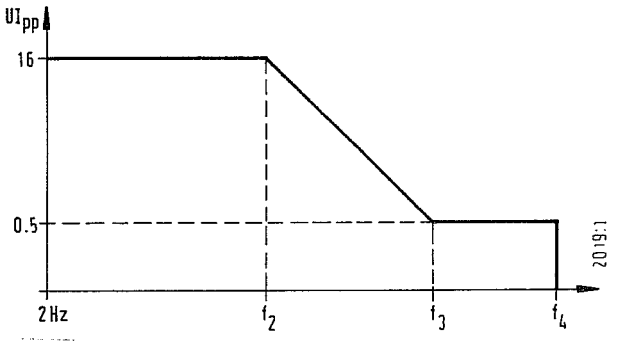
Pass band attenuation compensation ..... ± 1 dB

(The 2 Hz high pass- and 6.7 MHz low pass filters are also active in this operating mode).

1.4.1.2 Weighting filter combinations to CCITT Recommendation O.171 (3 dB cutoff frequencies)

Bit rate	Low pass filter	High pass filter 1	High pass filter 2
1544 kbit/s	74 kHz	10 Hz	8 kHz
2048 kbit/s	185 kHz	20 Hz	700 Hz
6312 kbit/s	300 kHz	10 Hz	24 kHz
8448 kbit/s	600 kHz	20 Hz	3 kHz
32064 kbit/s	1.2 MHz	60 Hz	160 kHz
34368 kbit/s	1.2 MHz	100 Hz	10 kHz
44736 kbit/s	6.7 MHz	10 Hz	900 kHz
139264 kbit/s	6.7 MHz	200 Hz	10 kHz

1.4.1.3 Maximum measurable jitter amplitude referred to the jitter frequency



Clock signal measurements
(input switch set to CLOCK)

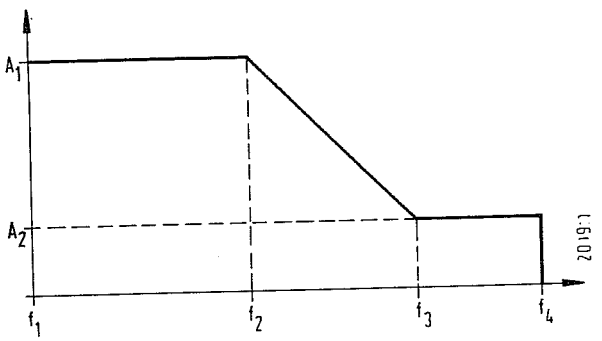
Bit rate Mbit/s	f_2 kHz	f_3 kHz	f_4
0.7 to 2	0.63	20	1/10 th
> 2 to 8	1.5	50	of the
> 8 to 168	7.8	250	bit rate

Data signal measurements
(input switch set to DATA)

Bit rate Mbit/s	f_2 kHz	f_3 kHz	f_4
0.7 to 2	0.063	2	1/10 th of the bit rate
> 2 to 8	0.25	8	$\geq f_4 \geq$ 1/100 of the bit
> 8 to 32	1.0	33	rate, depending on the
> 32 to 128	1.5	50	edge density of the
> 128 to 168	4.7	150	data signal

1.4.1.4 Guaranteed jitter measurement ranges

The quoted error limits are guaranteed for the jitter measurement ranges given below. The measurement is made on a clock signal with the input switch set to CLOCK.



Bit rate kbit/s	Jitter (UI_{pp}) A_1	A_2	Frequencies f_1	f_2	f_3	f_4
1544	10	0.3	10 Hz	200 Hz	7 kHz	40 kHz
2048	10	0.5	20 Hz	2.4 kHz	45 kHz	100 kHz
6312	10	0.5	10 Hz	1.6 kHz	32 kHz	160 kHz
8448	10	0.5	20 Hz	400 Hz[1)]	8.5 kHz	400 kHz
8448	10	0.5	20 Hz	10.7 kHz[2)]	200 kHz	400 kHz
32064	10	0.5	60 Hz	1.6 kHz	32 kHz	800 kHz
34368	10	0.5	100 Hz	1 kHz	20 kHz	800 kHz
44736	16	0.5	10 Hz	3.2 kHz	100 kHz	4.5 MHz
139264	10	0.5	10 Hz	500 Hz	10 kHz	3.5 MHz

1) for low Q systems

2) for high Q systems

1.4.3 JITTER DISPLAY

4 digit display ..... from 0 to 15.99 UI_{pp}

Resolution < 2 UI ..... 0.001 UI

$\geq$ 2 UI ..... 0.01 UI

Display averaging can be switched in, averaging time ..... 5 s

Positive or negative jitter amplitudes can be selected for display:

+p	positive peak value only
-p	negative peak value only
pp	peak-to-peak measurement

1.4.4 DISPLAYED JITTER ERROR LIMITS (to CCITT Recommendation O.171)

Measured using a clock signal or ...1000... pattern at 1 kHz jitter frequency and with internally generated comparator clock:

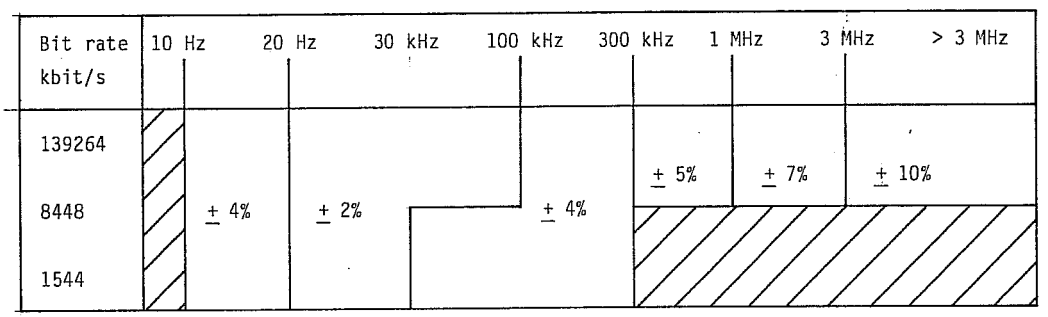
Filter	at bit rates	Error limits (AVERAGE mode)
internal	$\leq$ 30 Mbit/s	< 5 % of measured value $\pm$ 5 mUI_{pp}
	> 30 Mbit/s	< 5 % of measured value $\pm$ 10 mUI_{pp}
external	$\leq$ 30 Mbit/s	< 5 % of measured value + 7/-3 mUI_{pp}
	> 30 Mbit/s	< 5 % of measured value +17/-3 mUI_{pp}

Measured using pseudo random bit sequences at 1 kHz jitter frequency and with internally generated comparator clock:

Filter	at bit rates	Error limits (AVERAGE mode)
internal	$\leq$ 8448 kbit/s	< 5 % of measured value +18/- 9 mUI_{pp}
	> 8448 kbit/s	< 5 % of measured value +28/-12 mUI_{pp}
external	$\leq$ 8.448 Mbit/s	< 5 % of measured value +22/-3 mUI_{pp}
	> 8.448 Mbit/s	< 5 % of measured value +32/-3 mUI_{pp}

Maximum frequency response error:

Referred to a jitter frequency of 1 kHz, measured using a clock signal:



1.5 P H A S E H I T S

The demodulated jitter function signal is fed to a phase hit counter. The input of the phase hit counter has a threshold value circuit, the operating (nominal) point of which can be set as UI_p using the keypad. Every time this limit is exceeded, an event is counted and displayed; the event together with time-of-day information can be printed out if required. Depending on whether positive peak of negative peak jitter is displayed, the counter will register whether the positive or negative threshold has been exceeded:

Jitter display	Phase hit counted when
+ peak	positive threshold exceeded only
- peak	negative threshold exceeded only
peak-to-peak	either threshold exceeded

1.5.1 EVENT DISPLAY

ABSOLUTE COUNT	All phase hits exceeding the threshold value are counted over a gating time which is selectable. 6 digit display up to 999999, above this value 3 digit display plus exponent. Max. display value 1.99×10^9.
EVENT FREE SECONDS	The ratio of the number of periods of one second during which the thresholds were not exceeded to the total gating time is displayed in %.
RATIO	The ratio of the number of times the phase thresholds were exceeded to the number of seconds over a selectable time period is displayed. 3 digit display plus exponent.

1.5.2 PHASE THRESHOLDS

Value entered using the keypad

Range ..... 0.05 to 7.99 UI_p

Resolution ..... 0.01 UI

1.5.3 GATING TIME

Fixed periods selectable via menu ..... 1, 10, 100 or 1000 s

or variable periods, selectable using the keypad

in hours and minutes ..... up to 99 hours 60 minutes

or in days and hours ..... up to 99 days 24 hours

Or as a number of clock cycles selectable via menu ..... 10^6, 10^7, ..., up to 10^{12}

1.5.4 PHASE THRESHOLD ERROR LIMITS

Threshold setting ..... $\leq$ 2% of the threshold value plus the phase jitter meter error

Gating time error ..... $\leq 5 \times 10^{-5}$

1.6 CODE TRANSGRESSION COUNT

Evaluation for line codes ..... AMI, HDB3 and CMI

A plug-in module (option BN 2019/00.01) can be fitted to allow evaluation of 4B3T and 5B6B codes

EXTERN

The counter can be used for event counting of any type when set to EXTERN. Signal input is via a socket on the back panel.

The event display mode and the gating time are common to code transgression- and phase hit event counting, being selected at the same time. In RATIO mode, the displays for both code transgression- and phase hit counters are the same, although the results are calculated differently.

1.7 OTHER INPUTS AND OUTPUTS

1.7.1 PHASE DEMODULATOR OUTPUT*

Output impedance ..... 75 Ω

Return loss, up to 5 MHz ..... ≥ 30 dB

Output for 1 UI jitter amplitude ..... 0.1096 V

Error limits: see 1.4.

1.7.2 CONNECTIONS FOR LOOPING-IN EXTERNAL FILTERS

Connectors (back panel) ..... BNC sockets

Input/output impedances ..... 75 Ω

External filter nominal pass band attenuation ..... 6 dB

Pass band attenuation compensation (back panel control) ..... ± 1 dB

1.7.3 REFERENCE CLOCK OUTPUT (same as regenerated input clock)

Connector (back panel) ..... BNC socket

Output impedance ..... 75 Ω

Peak-to-peak output voltage (a.c. coupled) ..... 0.8 V

1.7.4 COMPENSATED OUTPUT SIGNAL TO PF-4

Automatic $\sqrt{f}$ compensation; compensation at 70 MHz up to ..... 12 dB

Connector (back panel) ..... BNC socket

Output impedance ..... 75 Ω

1.7.5 CODE TRANSGRESSION SIGNAL OUTPUT

A positive-going pulse is output each time a code transgression is detected

Pulse width ..... 0.5 UI

Connector (back panel) ..... BNC socket

Output impedance ..... 75 Ω

No load output signal level ..... ECL

1.7.6 CODE TRANSGRESSION SIGNAL INPUT

Any events can be counted using this input.

Connector (back panel) ..... BNC socket

Logic and input levels switchable

75 Ω referred to -2 V ..... ECL levels

10 kΩ referred to ground ..... LO = 0 to 0.3 V

HI = 1 to 5.0 V

10 kΩ referred to ground ..... TTL levels

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* Versacon® 9 basic 75 Ω connector fitted with BNC insert

1.8 <IEC 625>/IEEE 488 INTERFACE (option BN 958/21)

All operations of the PJM-4 are remote controllable. The results of measurements can also be read out, and the PJM-4 can control an IEC bus compatible printer via the controller function.

1.9 GENERAL SPECIFICATIONS

Power supply

Voltage selector setting	Nominal a.c. line voltage range
220 V	193 to 242 V
110 V	90 to 121 V

A.C. line frequency (nominal range for use) ..... 47.5 to 63 Hz
Power comsumption ..... 115 VA
Safety class, to VDE 0411 and IEC 348 I

Ambient temperature

Climate group ..... Ia
Nominal range for use ..... +5 to +40°C
for storage and transport ..... -40 to +70°C

Dimensions in mm

Bench model (w x h x d) ..... 477 x 155 x 434

Weight ..... approx. 16 kg

Ordering information

The following versions are available:

PJM-4 Jitter Meter — BN 2019/01
bit rates 2048, 8448, 25776, 34368 and 139264 kbit/s
panel and menu in English

PJM-4 Jitter Meter — BN 2019/02
as BN 2019/01 but with
panel and menu in German

PJM-4 Jitter Meter — BN 2019/03
bit rates 1544, 3152, 6312 and 44736 kbit/s
panel and menu in English

PJM-4 Jitter Meter — BN 2019/04
bit rates 1544, 3152, 6312, 32064 and 97728 kbit/s
panel and menu in English