LOGIC ANALYZERS

Ultra-High Speed State and Timing Analysis Modules

HP 16517A and HP 16518A

- Trigger directly on setup and hold violations down to 2.0 ns.
- Make timing measurements across as many as 80 channels with the resolution and precision of an oscilloscope.
- Characterize the performance of a high-speed ASIC or target system.
- Capture the most complex problems with an easy to use trigger macro library.

HP 16517A/16518A High-Speed State and Timing Modules

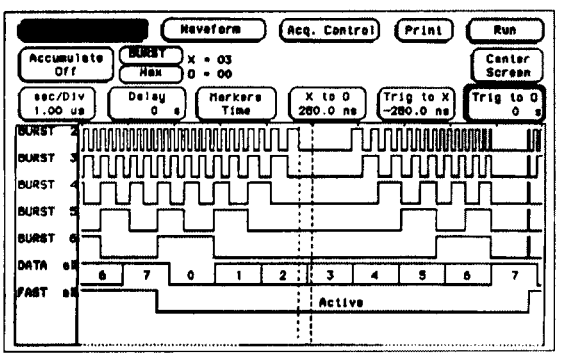
Key Specifications and Characteristics

	HP 16517A/16518A
Maximum timing speed	2 GSa/s or 4 GSa/s[1]
Maximum state speed	1 GSa/s 1 or 2 GSa/s[2]
Memory depth	64 K or 128 K[1]
Channels per card	16/16[3]
Probe input R&C	0.2 pF, then through 500 Ω, 3 pF and 100 Ω k
Trigger macro library	Yes, with 4 sequence levels
Channel-to-channel skew	250 ps, typical

[1] Half-channel mode doubles memory depth and doubles timing speed.
[2] Maximum state speed with oversampling.
[3] HP 16518A expansion card requires HP 16517A master card. Up to four HP 16518As are supported by each HP 16517A.

Find the Cause of Elusive Problems

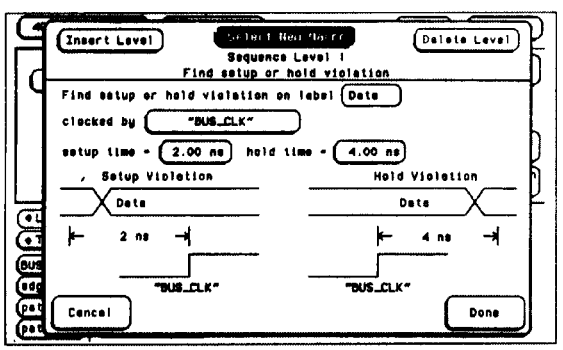
The 64-K deep memory lets you capture data over many clock cycles while retaining the highest multi-channel accuracy ever in a logic analyzer. Verify the timing of critical edges with 250-ps resolution across up to 40 channels, or 500-ps resolution, across up to 80 channels. Use the 1-GSa/s synchronous state analysis to view high-speed data streams across up to 80 channels.



Capture 32 μS of circuit activity while maintaining 250-ps resolution.

Precisely Characterize Setup or Hold Times

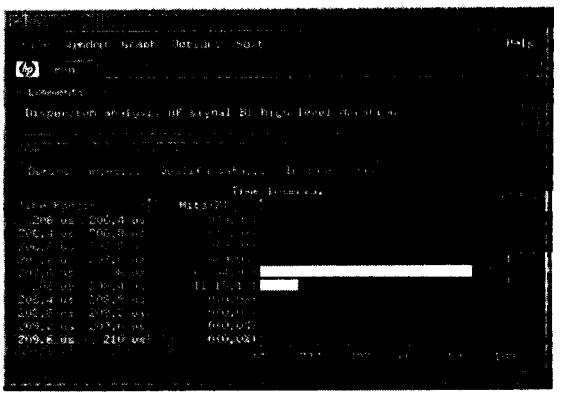
The 250-ps precision (channel-to-channel skew) allows this logic analyzer to be used in place of an oscilloscope for characterization. The high-channel count of a logic analyzer improves the efficiency of the characterization process.



A graphical trigger macro library ensures fast trigger condition setups.

Profile Your High-Speed Measurements with the HP 16505A Prototype Analyzer

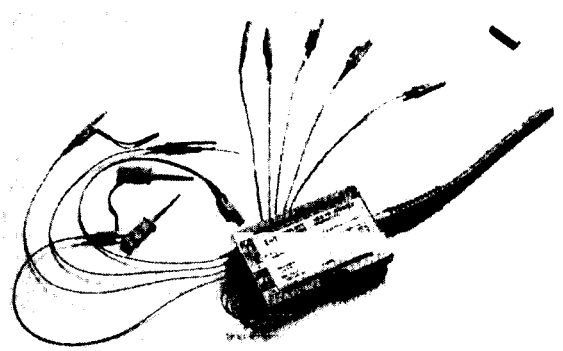
The time-interval tool of the HP 16505A's SPA tool set can be used to verify signal timing specifications. The time-interval tool measures the distribution of time between two user-defined events. The tool can be used to measure setup and hold times, the jitter between two edges or the variation between two bus states. Accumulate mode can be used to analyze the behavior of your system over a long period of time. Statistics, such as the maximum time, minimum time, standard deviation and mean, help you document system behavior.



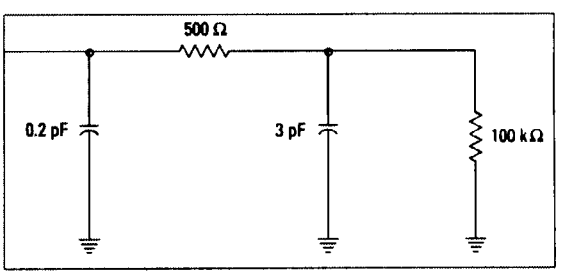
Visually verify signal timing specifications.

Flexible High-Speed Probing

HP has developed special active probe pods to meet the needs of ultra-high speed timing measurements. Lightweight probe leads can attach to the target system via a variety of probing adapters. The probe loading of the target system is kept to a bare minimum by the use of an innovative RC circuit.



Flexible probe options allow you to get the measurement you need.



HP 16517/18A Probe load equivalent circuit.

Key Literature

Technical Specifications for HP 16517A, HP 16518A State and Timing Card, p/n 5091-7216E
4-GSa/a and 1-GSa/s Synchronous State for the HP 16500 Logic Analysis System, p/n 5091-8096E