

# LOGIC ANALYZERS

## State and Timing Analysis Modules

HP 16550A, 16554A, 16555A, 16556A, 16555D, 16556D



### Key Specifications and Characteristics

	HP 16550A	HP 16554A <sup>1</sup>	HP 16555A/16555D <sup>1</sup>	HP 16556A/16556D <sup>1</sup>
<b>Timing-analysis rate</b>	Conventional: 250/500 MHz <sup>2</sup> Transitional: 125/250 MHz <sup>2</sup> Glitch: 125 MHz	Conventional: 125/250 MHz <sup>2</sup>	Conventional: 250/500 MHz <sup>2</sup>	Conventional: 200/400 MHz <sup>2</sup>
<b>State-analysis rate</b>	100 MHz	70 MHz	110 MHz <sup>3</sup>	100 MHz
<b>Channels/card</b>	102	68	68	68
<b>Channels/timebase</b>	204	204	204	340
<b>Memory depth/channel</b>	4 K/8 K <sup>4</sup>	512k/1024K <sup>4</sup>	1M/2M <sup>4</sup> , 2M/4M <sup>4</sup>	1M/2M <sup>4</sup> , 2M/4M <sup>4</sup>
<b>Setup/hold time</b>	3.5/0 ns to 0/3.5 ns adj. in 500 ps steps	3.5/0 ns to 0/3.5 ns adj. in 500 ps steps	3.5/0 ns to 0/3.5 ns adj. in 500 ps steps	3.5/0 ns to 0/3.5 ns adj. in 500 ps steps
<b>Minimum detectable glitch</b>	3.5 ns	3.5 ns	3.5 ns	3.5 ns
<b>Probe input R and C</b>	100k $\Omega$ and ~ 8 pF	100k $\Omega$ and ~ 8 pF	100k $\Omega$ and ~ 8 pF	100k $\Omega$ and ~ 8 pF
<b>Triggering terms</b>	Patterns: 10; Ranges: 2; Edge and glitch: 2; Timers: 2	Patterns: 10 <sup>5</sup> ; Ranges: 2; Edge and glitch: 2; Timers: 2	Patterns: 10 <sup>5</sup> ; Ranges: 2; Edge and glitch: 2; Timers: 2	Patterns: 10; Ranges: 2; Edge and glitch: 2; Timers: 2
<b>Trigger sequence levels</b>	12 in state and 10 in timing	12 in state and 10 in timing	12 in state and 10 in timing	12 in state and 10 in timing
<b>Symbols</b>	Unlimited	Unlimited	Unlimited	Unlimited

<sup>1</sup>HP 16554A, 16555A, 16555D, 16556A, and 16556D can only be used with the HP 16500B or 16500C logic analysis mainframe.

<sup>2</sup>Half-channel mode doubles memory depth, doubles maximum conventional timing speed and doubles maximum transitional timing speed.

<sup>3</sup>For 110-MHz mode only—Single clock edge with qualifiers. 100-MHz mode and below is the same as the HP 16550A.

<sup>4</sup>Memory depth doubles in half-channel timing mode.

<sup>5</sup>Eight pattern recognizers are available in HP 16554A timing modes and HP 16555A/16555D timing and 110-MHz state analysis modes.

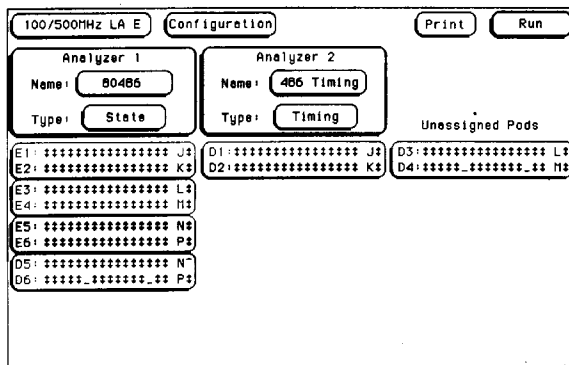
### State and Timing Analysis with a Choice of Depth

The HP 16550 series of state and timing analyzers offers a range of memory depths and state analysis speeds to fit your application. The HP 16550A offers industry-standard state and timing analysis features at an affordable price. The HP 16554A, 16555A, 16556A, and the new HP 16555D and 16556D analyzers provide the same acquisition and triggering capabilities as the HP 16550A, but provide the deeper memory needed to capture elusive system crashes.

All HP 16550 series analyzers use the same probing scheme, which makes it possible for you to easily interchange probing interconnections whenever your probing needs change. All HP 16550 series analyzers also connect to Hewlett-Packard's broad and growing selection of preprocessor solutions because the probes are compatible with previous HP state and timing analyzer modules.

### Capture State or Timing Data on All Channels

With the HP 16550 series of state and timing analyzers, there is no need to connect special probes to view timing activity. All channels on HP state and timing analysis modules perform either state or timing functions. Set up your HP 16550 series analyzer to perform simultaneous, fully time-correlated state analysis on some channels, and timing analysis on the rest.



Assign channels to capture state timing data without moving probes.

### Advanced Trigger Macro Capture Elusive Problems

Both basic and complex state and timing macros are available in the trigger macro library. Macros can be combined to create custom trigger setups.

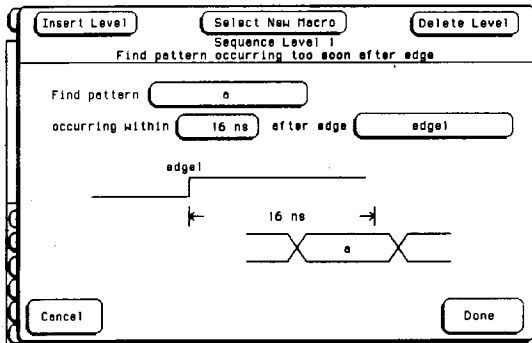
Macro Type	Trigger Macro	Internal Levels Used
	+ MORE +	
Basic	1. Find anystate n times	1
Macros	2. Find pattern present/absent for > duration	1
	3. Find pattern present/absent for < duration	4-5
	4. Find edge	1
	5. Find Nth occ. of an edge	1
Pat/Edge	1. Find edge within a valid pattern	2
Combs	2. Find pattern occurring too soon after edge	3-4
	3. Find pattern occurring too late after edge	2
Time	1. Find 2 edges too close together	3-4
Violations	2. Find 2 edges too far apart	2
	3. Find width violation on a pattern/pulse	4-5
	+ MORE +	
Cancel		Internal Levels Remaining = 10
		Done

The HP 16550 series timing trigger macro library.

Each trigger macro has a graphic of the measurement and a sentence-like structure to make triggering easy. Set up your triggering in terms of the measurement you want to make, rather than in terms of the trigger functions in the logic analyzer.

Families of trigger macros make it easy to pick out just the trigger macro you need, and avoid the hassle of wading through a long list of triggers to find the one you want. Families of trigger macro measurements include:

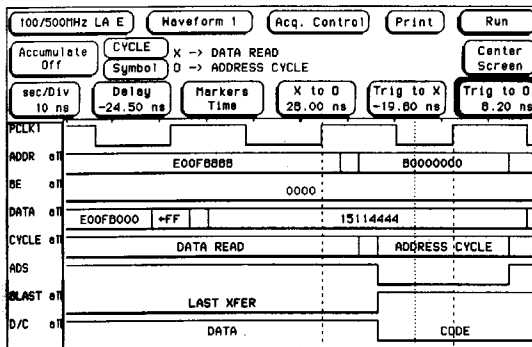
- Basic macros, including find anystate n times;
- Sequence-dependent macros, including find a n-bit serial pattern;
- Time-violation macros, including find an event 2 occurring too soon after event 1.



Typical timing trigger macro input screen.

### Analyze Distant Timing Events with Transitional Timing

Capture events that are seconds apart while maintaining 4-ns resolution with the HP 16550A. Transitional timing samples at full speed but only stores data when a transition occurs. This technique effectively extends the total time captured by the acquisition memory while maintaining high time resolution.



Display timing measurements with bus values overlaid in the waveforms.

### Track Problems in Multiprocessor and Multiple Bus Systems

Configure your HP 16550 series logic analyzer as two independent state analyzers that sample data using separate clocks. Time tagging of states lets you time-correlate and view the state listing interleaved on the same screen.

Label>	HPID	Time	HPID	DATA (103118 BP Probe)
Base>	ASCII	Absolute	Hex	68000 Hexmonics / Hex
8	D	3.509 ms		xx44 user data write
9	I	4.089 ms	44	xx49 user data write
10	S	4.678 ms	49	xx53 user data write
11	K	5.268 ms	53	xx48 user data write
12	K	5.859 ms	48	xx20 user data write
13	D	6.438 ms	20	xx44 user data write
14	I	7.026 ms	44	xx49 user data write
15	R	7.618 ms	49	xx52 user data write

View interactions between two separately clocked systems.

### Capture Up to 340, 2M Deep Channels Simultaneously

Use the new HP 16555D and 16556D and the 16554A, 16555A and 16556A to debug ASICs, 8-bit, 16-bit, 32-bit and 64-bit microprocessors. Connect five HP 16556D cards for 340-channel wide measurements. The HP 16555D and HP 16556D provide 2M of acquisition memory across all channels. The HP 16555A and 16556A provide 1M of acquisition memory while the HP 16554A provides 512K.

The memory depth of all cards is doubled in timing analysis half-channel mode.

To have a Hewlett-Packard representative help you place an order or to get more information call 1-800-452-4844

### Find Intermittent Errors Using Postprocessing

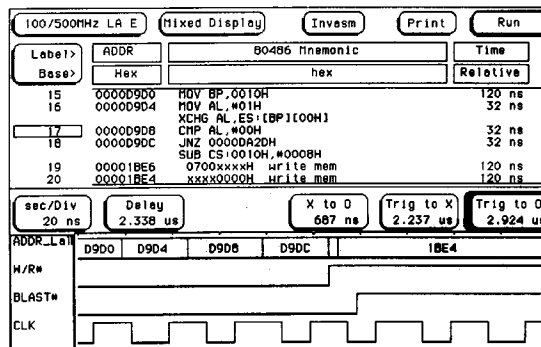
In state mode, set up compare mode to "run until compare not equal" to capture intermittent errors. Use compare for quick go/no-go testing of your product in manufacturing. State compare shows you the effects of system changes by comparing each sample in the current measurement to each sample in the previous measurement. In timing mode, capture intermittent setup and hold violations using the specify-stop-measurement feature to repetitively acquire data until the time interval between two patterns violates a specified condition.

### Enhance Troubleshooting with Flexible Display Modes

State and timing analyzers let you display state measurements in listings, X-Y chart, or state waveforms. In addition to the waveform display, the HP 16550A, 16554A, 16555A/D, and 16556A/D allow you to display timing information as a listing. Markers placed on one display are automatically updated in the other display modes.

### Find Whether the Problem is in Software or Hardware

Arm the timing analyzer with the state analyzer to capture system behavior between states. Display both measurements on one screen and use time-correlated markers to identify the cause of problem states.



Display time-correlated state and timing measurements on the same screen.

### Analyze Your Software with Informative Listings

New technology allows you to filter the disassembled trace, so it's easier to analyze. For example, suppress the display of instructions that were prefetched, but not executed. Display your high-level symbols in the state listing. If you program in a high-level language, the optional HP E2450A symbol utility lets you import symbols from source code. The utility reads industry-standard object module formats.

Label>	ADDR	Symbol	Hexmonics/Hex
Base>			
4212	:get_message+006C	CO MOV AX, [BX+0154]	
		C4 MOV BX, [BP+06]	
		C7 MOV [BX+10], AX	
4214	:get_message+0074	CA MOV AX, #0014	
		CD INUL WORD PTR [BP+04]	
4216	:get_message+007C	DO MOV BX, AX	
		D2 MOV [BX+0142], #0000	
4219	:get_message+0084	DB POP SI	
		D9 POP DI	
		DA MOV SP, BP	
		DC POP BP	
		DD RET NEAR	
4235	display_req+0024	D4 JLE display_+00000010	
		D6 ADD [SI+03], CH	
4237	display_req+002C	D2 JNP display_+0000003D	
		DC MOV AX, #0002	

Disassembly filters let you analyze software from multiple viewpoints. The symbol utility lets you import and display symbols from your software.

### Key Literature

A Family of State and Timing Analyzers for the HP 16500C Logic Analysis System, p/n 5962-7245E